Application Note: Low Power & Standby Modes In Apex

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1 Purpose

The purpose of this document is to describe how to use the low power operating mode, standby mode and watchdog mode on the AN231E04.

2 Low Power Operating Mode

AnadigmDesigner2 (AD2) does not support low power mode for Apex devices (AN231E04), nevertheless there is a low power mode built into the silicon. To set a device into low power mode one must send a simple reconfiguration to the device as follows:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF5, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

The data above is represented in a format that would be written in a C-code application. To send this reconfiguration from AD2, put the data into a text file in the form of a column with one byte per column without the "0x" prefixes. Save this text file and rename the extension .AHF, then go to the "Configure" menu in AD2 and select "Write AHF File to Serial Port", then browse to the file just created and click on "Open".

To put the device back into normal power mode, send the following reconfiguration data:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF1, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

Low power mode reduces the power consumption to approximately 20% of what it would be in normal mode. To do this all opamp bias currents are significantly reduced, this has the effect of slowing down the OpAmps and reducing the bandwidth. The opamps have an 80MHz open loop gain at full bias, reducing their bias currents means the bandwidth is approximately 10MHz because the lower bias current slows the capacitor charge time and reduces the switched capacitor bandwidth/accuracy trade off. Low power is intended to be used for circuits with operating bandwidths in the audio range (d.c. to 20kHz), within this bandwidth no difference in performance will be observed.

At higher bandwidths, using low power mode the CAMs will all function but may not meet the 1% accuracy specification. Reason: the capacitor internally may not charge to 99.9%, this will have the effect of reducing gain slightly and allowing filter corner frequencies to be a little high. This cannot be specified exactly but theoretically the degradation, if one uses the device this way, will be repeatable.

3 Standby Mode

AnadigmDesigner2 (AD2) does not support standby mode for Apex devices (AN231E04), nevertheless there is a standby mode built into the silicon. In this mode there will be no analog functionality and the device will consume very little power.To set a device into standby mode one must send a simple reconfiguration to the device as follows:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0x00, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

The data above is represented in a format that would be written in a C-code application. To send this reconfiguration from AD2, put the data into a text file in the form of a column with one byte per column without the "0x" prefixes. Save this text file and rename the extension .AHF, then go to the "Configure" menu in AD2 and select "Write AHF File to Serial Port", then browse to the file just created and click on "Open".

To put the device back into normal power mode, send the following reconfiguration data:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF1, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

Standby mode shuts down all of the analog circuitry and reduces the power consumption to approximately 0.3mA. To reduce the power consumption further, stop ACLK. With ACLK stopped and all analog circuits disabled, the power consumption will be approximately 4uA.

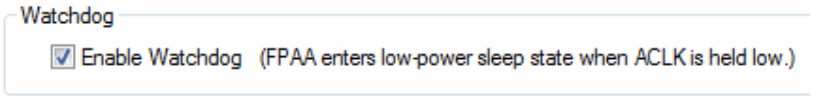
Note that it is perfectly acceptable to switch between low power mode and standby mode. To switch from standby mode back into low power mode, use the following reconfiguration data:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF5, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

4 Watchdog Mode

AnadigmDesigner2 (AD2) does support watchdog mode for Apex devices (AN231E04). To enable watchdog mode from AD2, go to the Settings menu and select “Active Chip Settings…”. Alternatively just double click over the chip. Now select the Chip tab and check the box labelled “Enable Watchdog” (as shown below).



Watchdog mode is an automatic power savings feature. When enabled, the Watchdog circuit monitors the frequency of the primary analog clock (ACLK pin). When ACLK falls below 31.25 KHz, the device will automatically shift into a powered-down condition. Resumption of ACLK will immediately bring the part back up into a normal powered state, though how fast normal signal processing resumes is a function of the current CAB configurations. In the powered down condition, all of the analog circuitry is disabled and the device should consume approxiimately 4uA of current.

An alternative method of setting watchdog mode is by sending a simple reconfiguration to the device as follows:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF3, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

The data above is represented in a format that would be written in a C-code application. To send this reconfiguration from AD2, put the data into a text file in the form of a column with one byte per column without the “0x” prefixes. Save this text file and rename the extension .AHF, then go to the “Configure” menu in AD2 and select “Write AHF File to Serial Port”, then browse to the file just created and click on “Open”.

To turn watchdog mode off and put the device back into normal power mode, send the following reconfiguration data:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF1, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

Or to turn watchdog mode off and put the device back into low power mode, use the following reconfiguration data:

```
0xD5, 0x01, 0xC1, 0x91, 0x00, 0x01, 0xF5, 0x2A, 0x00
```

***NOTE**: the second byte is the device address which in this case = 1*

5 Settling Times

These circuit updates will occur in the same way as all circuit updates occur within half a clock cycle (ACLK) following the transfer of data from shadow RAM to main RAM (the RAM transfer signal rising edge). The change in power (OpAmp bias current) will settle in less than half of one ACLK cycle.

The settling time associated with the performance of a specific circuit will depend entirely on that circuit, for example Filters have a 1/Fc setting time, so the lower the corner frequency the longer the settling time. FPAA settling time can be considered the same (and will be the same or better than) conventional analog circuit step response settling time.

There is too much variability, choice of circuits and parameters for us to publish generic estimates; it is a simple case of trying it with your own circuit.