ANADIGM AnadigmFilter 1 Control Interface (16 Bit Configuration Word)

Gain Settings			Analog Input Pin settings		Filter Topology		Filter approximation		DivisorB *Internal Clock divider settings, (divider to scale Fc in octave steps)*				DivisorA *Filter Fc settings (9% steps across octave)*		
MSB															LSB
G3	G2	G1	I2	I1	T4	T3	T2	T1	B4	B3	B2	B1	A3	A2	A1
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19

G3,G2,G1	Gain (dBs)
000	-infinity (Mute)
001	0.0
010	3.0
011	6.0
100	9.0
101	12.0
110	15.0
111	18.0

I2,I1	Active input(s)
00	None
01	Input A
10	Input B
11	A & B *Note1*

T4,T3	Filter topology
00	Lowpass
01	Highpass
10	Bandpass
11	Bandstop

The Filter Approximation applied depends upon the Filter topology selected.

See Table insert to the lower left

B4,B3,B2,B1	DivisorB
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

A3,A2,A1	DivisorA
000	1.0
001	0.917
010	0.841
011	0.771
100	0.707
101	0.648
110	0.595
111	0.545

Filter Approximation Applied		T4,T3	T2,T1	Comment	Width	Limits (FCLK = ACLK / DivisrB)
Lowpass	Butterworth	00	00		n/a	Max Fc = 400kHz @ FCLK(max) = 8MHz
Lowpass	Chebyshev	00	01		n/a	Max Fc = 500kHz @ FCLK(max) = 10MHz
Lowpass	Bessel	00	10		n/a	Max Fc = 250kHz @ FCLK(max) = 5MHz
Lowpass	Bypass	00	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Highpass	Butterworth	10	00		n/a	Max Fc = 60kHz @ FCLK(max) = 6MHz
Highpass	Chebyshev	10	01		n/a	Max Fc = 100kHz @ FCLK(max) = 10MHz
Highpass	Bessel	10	10		n/a	Max Fc = 50kHz @ FCLK(max) = 5MHz
Highpass	Bypass	10	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Bandpass	Inverse Chebyshev	01	00	narrow	10%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	01	01	narrow	10%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandpass	Inverse Chebyshev	01	10	wider	40%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	01	11	wider	40%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandstop	Inverse Chebyshev	11	00	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	01	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Inverse Chebyshev	11	10	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	11	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz

Notes

1) If inputs A and B are selected then the two active input signals will be summed.

2) Setting of five 0's for the control bits C[15:11] (zero gain and no inputs selected) causes the FPAA to be reset and AnadigmFilter to go into standby (approx 6mA from 3.3volts)

3) Max Fc, or maximum Filter Corner or Center Frequency limits have been determined for better than 1% accurate filter parameters, exceeding these limits will result in loss of filter accuracy.

*4) Bypass filter approximation provides a flat response from d.c. to FCLK * 0.1. (FCLK = ACLK / Divisor_B). Divisor_A inputs have no effect in this mode, gain and input select still apply.*

5) Divisor_A step size is mathematically equal to (8thsqrt(2))/8. or ((2)^^(1/8))/8.