Application Note: IQ Filtering in an RFID Reader Using Anadigm Integrated circuits,

Rev: 1.0.3

Date: 3rd April 2006

We call this multi-chip circuit solution “RangeMaster3”,

It uses Anadigm’s. RangeMaster2 integrated circuits (2 x AN238E04 and 1 x AN238C04).

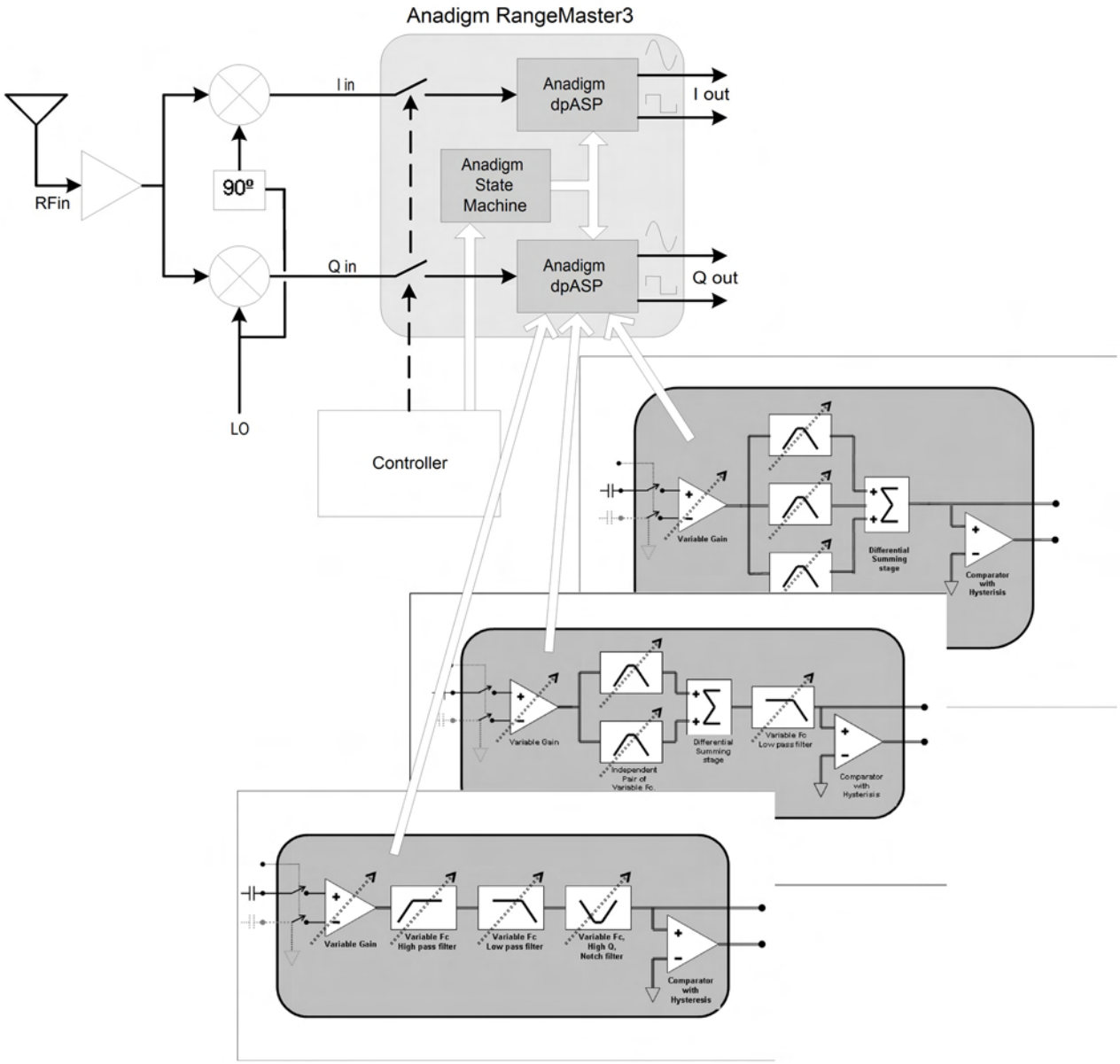

TABLE OF CONTENTS

Document revision 1.0.3, 3rd April 2006
Author: Dave Lovell
Doc No. AP0238K2-U001a

1 Purpose

This document describes the benefits of using an Anadigm RangeMaster3 programmable analog baseband processor to process the demodulated I and Q channels in an RFID tag reader. Filter frequencies can be simply and quickly programmed to allow the user to create a universal reader that supports multiple standards, providing full support for EPC Global Gen 1/ Gen 2 (Class 0,1,2) and ISO18000-6 protocols. In addition, gain and balance can be adjusted to optimize the range and sensitivity of the reader, and background interference can be notched out. The Rangemaster3 chipset also has a low current standby mode, and a pin that allows fast disconnection of the inputs for anti-saturation purposes.

References:

RangeMaster2 Datasheet

RangeMaster2 Evaluation Board Quick Start Guide

www.anadigm.com

2 Introduction

The problems associated with creating a radio frequency identification (RFID) reader include:

1. A multitude of standards and protocols that are under constant revision, and unpredictable shifting in popularity between them.
2. Installation issues – a reader has to cope with a variety of environments, background noise and interference from say fluorescent lights.
3. Variable read range – a reader has to cope with different tag ranges. Ideally a reader should be dynamically adjustable with no signal interruption in order to optimize performance.
4. Saturation of input filters while transmitting – the reader needs to be able to quickly disconnect it's receive channel filters to avoid them going into saturation from which they might be slow to recover.

The Anadigm RangeMaster chipset is a programmable analog signal processor that provides a single solution to all of these problems.

RangeMaster is a chip set comprising one or more Anadigm dpASP (dynamically programmable Analog Signal Processor) chips with an Anadigm RFID state machine. It is designed for processing the demodulated baseband signals in an RFID reader. Any number of dpASPs can be identically programmed in parallel by the state machine with no increase in programming time or delay. This allows for the processing of multiple channels, such as the I and Q demodulated channels in an RFID tag reader.

The advantages of using a programmable analog signal processor is that a single universal reader can be created that can be customized to read different RFID tag types, with different modulation types and frequencies. The RangeMaster family fully supports HF and UHF protocols – EPC Global Gen 1 and Gen 2 (class 0, 1, 2) and ISO18000-6 standards.

Furthermore, RangeMaster allows fast programming of gain and balance for optimum performance over a variety of tag ranges, notch frequency for removal of background interference, and input switches for protection of filters against saturation during transmit.

NOTE: RangeMaster3, which is the subject of this document, is a 3-chip solution designed for processing the I and Q channels in an RFID tag reader. Note that RangeMaster3 is functionally equivalent to RangeMaster2, differing only in the fact that it has one more dpASP than RangeMaster2. The method of programming RangeMaster3 is identical to that for RangeMaster2 (see section 4).

3 RFID Reader Circuit

An RFID Reader works by first transmitting information to a tag by modulating an RF signal, typically in the range 860MHz – 960MHz. The tag receives both information and operating energy from this RF signal, and then responds by modulating the reflection coefficient of its antenna, thereby backscattering an information signal to the interrogator. The reader has to transmit a continuous-wave signal to the tag in order to receive the tag's response. This means that the reader has to extract small low frequency modulations from the large high frequency transmit signal. It does this by mixing a reference signal, which is the un-modulated transmit carrier signal, with the receive signal to cancel out the transmit frequency, leaving just the modulation frequencies. An example of such an RFID reader is shown in figure 1.

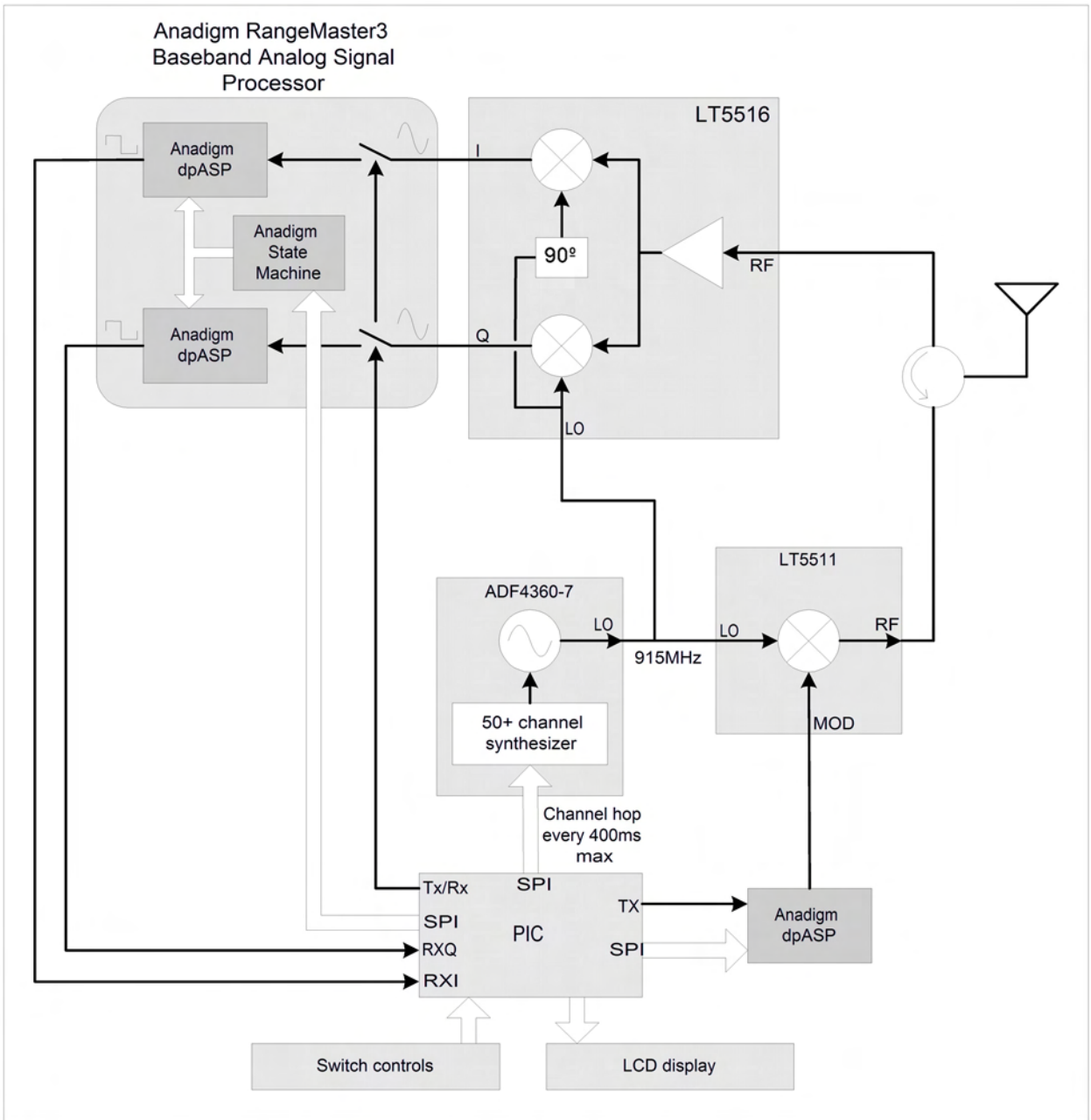

Figure 1: RFID Reader block diagram

The System Controller

In figure 1, the system controller of the RFID reader is a PIC. This performs the following functions:

1. Takes instructions from an external interface such as switches or keypad, and display information to the user.
2. Controls the channel hopping – there are regulations that demand that a reader must randomly channel hop between a set of carrier frequencies at regular intervals. In the US the regulations (FCC Part 15.247) demand channel hopping using a minimum of 50 channels with a maximum dwell time of 400mS. In figure 1 an ADF4360-7 provides the 915MHz carrier signal with multiple channels controlled by the PIC via a serial interface..
3. Sends the tag identification information by sending data to an Anadigm dpASP used to convert the data into an analog signal which is then mixed with the carrier using an LT5511 up-converting mixer. The dpASP would be configured by the PIC controller.
4. Send out a signal that opens the RangeMaster3's anti-saturation input switches during transmit and closes them during receive.
5. Program RangeMaster3 according to the desired filter frequencies, gain, balance, and notch frequency.
6. Receive the I and Q signals out of RangeMaster3 from its digital outputs.

3.1 IQ Demodulation

In figure 1, the receive signal demodulator is shown as an LT5516. This circuit takes a reference oscillator which in this case is the 915MHz generated by the ADF4360-7. It then mixes the received signal with this reference oscillator to reproduce the modulation signal. Since it is possible to get a zero signal out of a mixer by sampling the received signal at a zero crossing, 2 mixers are used in the LT5516 down-converting mixer, each using a version of the reference oscillator that is 90º out of phase with respect to the other. This ensures that at least one of the mixer outputs has acceptable amplitude. These 2 mixer outputs are called I and Q channels.

3.2 IQ Channel Filtering

The "I and Q" outputs from the IQ demodulator need to be filtered to remove spurs, harmonics and unwanted modulations. The RangeMaster3 chipset provides an ideal solution for this because 2 dpASP programmable filters can be programmed in parallel by a single state machine with no additional overhead in terms of programming time. Figure 2 shows a block diagram of the RangeMaster3 3-chip set solution for IQ filtering. In this example, the dpASP chips are shown with twin bandpass filter circuits. Section 3 contains a complete description of the digital interface.

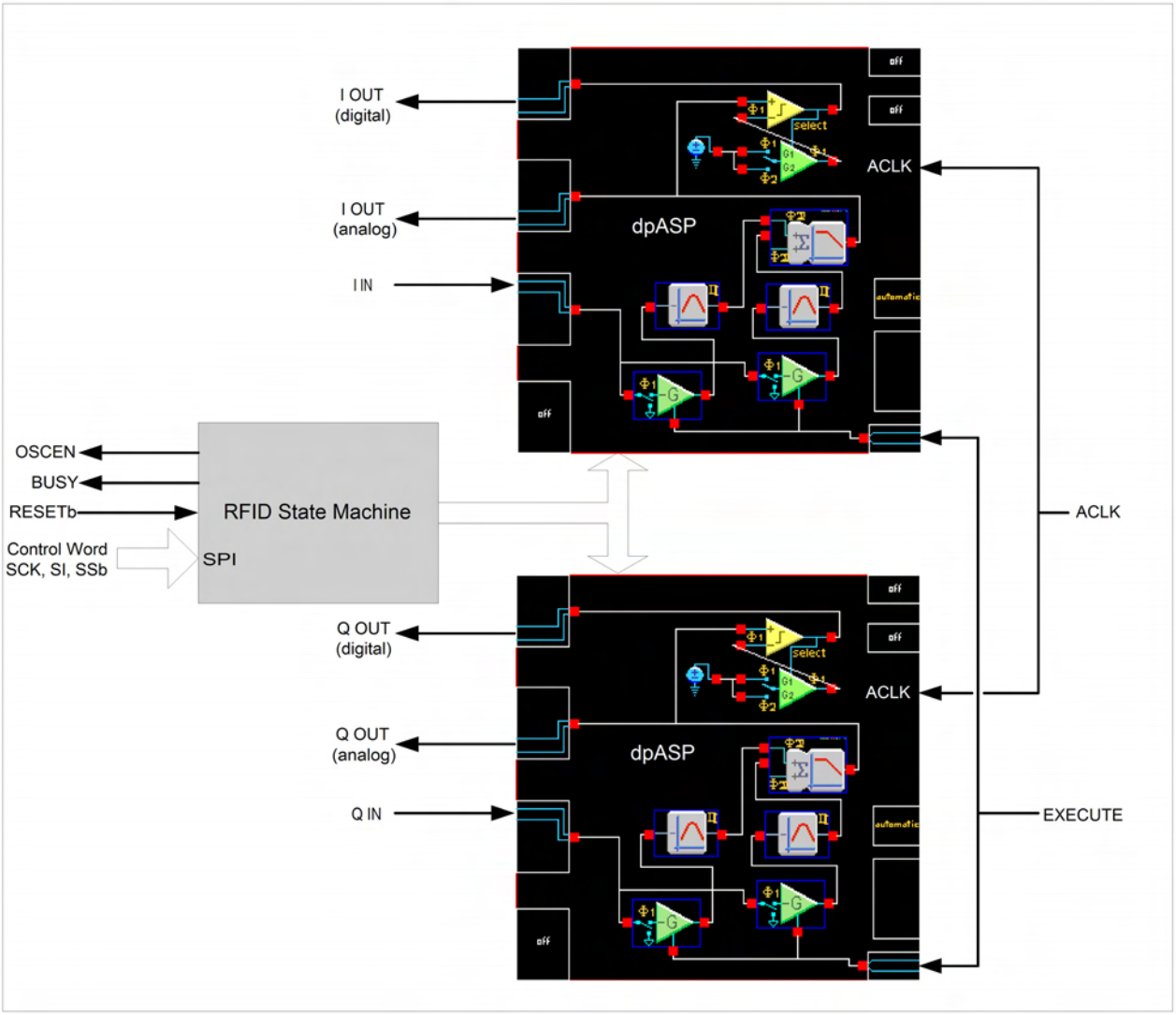

Figure 2: RangeMaster3 3-chip IQ Processor with twin bandpass filters

3.3 Programming the RangeMaster3 Filters

Using a simple 16 bit serial interface to the state machine (see section 3), it is possible to configure the dpASPs to process the I and Q channels for a wide variety of RFID standards. A choice of primary circuits can be downloaded into the dpASPs in parallel. These primary circuits are shown in figure 3a,b,c and consist of a twin bandpass filter, a triple bandpass filter, or a wideband filter with optional notch filter for removing unwanted interference from, for example, fluorescent lights.

The filter corner or centre frequencies can then be adjusted on the fly with no interruption to the analog signals through the filters. Filter frequencies can be varied over a wide range from 2kHz up to 848kHz, and in addition there is a class 0 circuit that provides twin bandpass filtering at 2.2MHz and 3.3MHz. Table 3 in section 3 shows the range of corner frequencies that can be programmed into RangeMaster3.

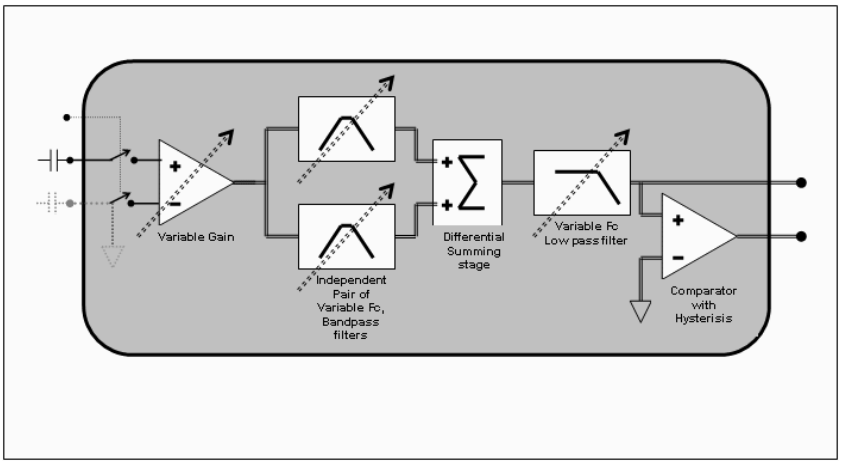

Figure 3a: Twin bandpass filter

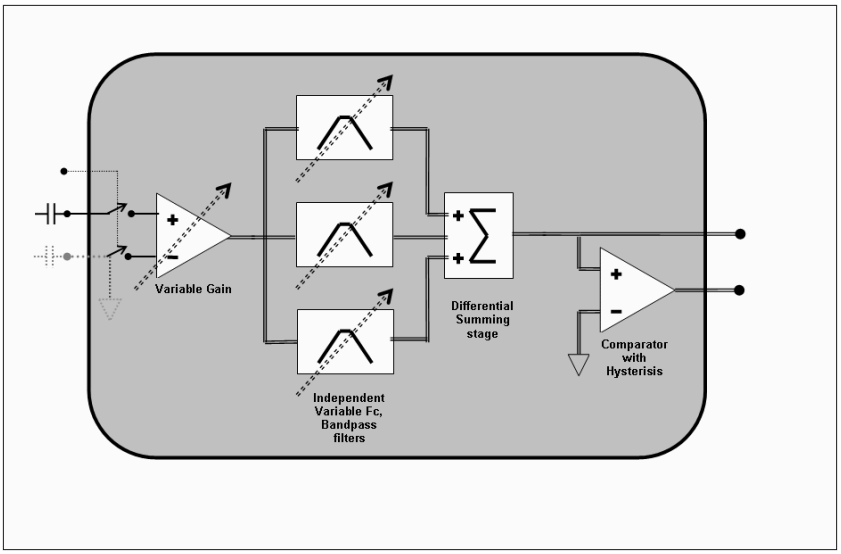

Figure 3b: Triple bandpass filter

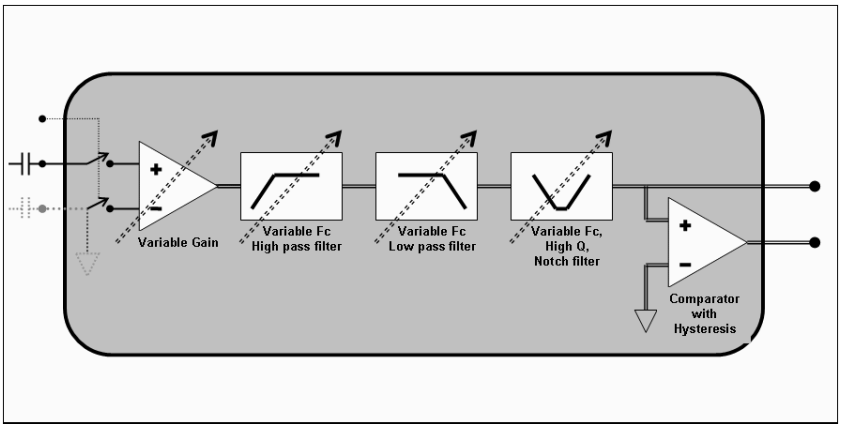

Figure 3c: Wideband filter with notch

Document revision 1.0.3, 3rd April 2006
Author: Dave Lovell
Doc No. AP0238K2-U001a

3.4 Programming the Notch Filter

For the wideband filter circuit, a notch filter is provided that can be programmed to notch out background interference of 50kHz, 52kHz or 54kHz. This filter can also be bypassed under program control if it is not required.

3.5 Programming Gain and Balance

In order to optimize the sensitivity of the reader in any environment, RangeMaster3 allows for the adjustment of gain from 0dB to 30dB using the input gain stage (figure 3a,b,c) and adjustment of balance in the bandpass filter circuits from 0dB to 12dB using the summing stage. See table 3 for the full range of values for gain and balance.

3.6 Anti-Saturation Switching

RangeMaster3 provides a pin for instant disconnection of the filter inputs for protection against saturation while the reader is transmitting. When the EXECUTE pin is taken high, a switch in the input to the filter circuit is opened. The maximum time for this input switch to open is 250nS. Figure 4 shows the output of the input stage when the EXECUTE pin is pulsed high. The output stops transmitting a signal within 250ns and goes to VMR (+1.5V).

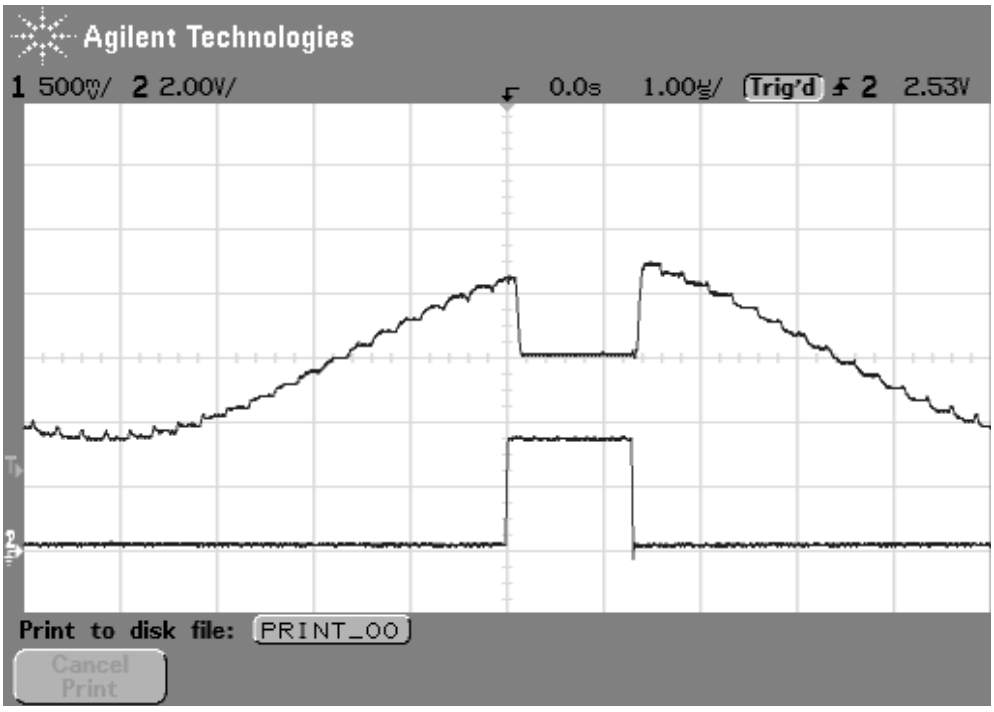

Figure 4: Anti-saturation switching

4 Digital Interface

4.1 Control Signals

Table 1 shows a description of the RangeMaster3 control signals shown in figure 2.

Signal	Type	Function
RESETb	I/P	Resets both the dpASP and state machine, active low
ACLK	I/P	External clock for dpASP (note 1)
EXECUTE	I/P	Anti-saturation input, disconnects filter inputs when high
SSb	I/P	Sync for configuration, active low, drive high at start & end of configuration & in between the bytes, drive low during the bytes (section 4.2)
SCK	I/P	Clock for configuration, clocks in data on rising edge (section 4.2)
SI	I/P	Data for configuration, must be valid about rising edge of SCK (section 4.2)
BUSY	O/P	This output goes high when the configuration state machine is busy. New configurations should not be started when BUSY is high.
OSCEN	O/P	This output is normally high but goes low when the state machine goes into standby. It can be used to enable/disable an external oscillator (note 2)

Table 1: Control Signals

Notes:

1. If ACLK is stopped then the dpASP will automatically go into standby mode.
2. The state machine can be put to sleep using configuration (table 3). If the OSCEN pin is connected to the enable pin of an oscillator module supplying ACLK, then the oscillator will be disabled when the state machine is put to sleep. This will cause ACLK to stop which will cause the dpASP to automatically go into standby mode. The next dynamic configuration will wake the state machine up which will enable the oscillator which will wake up the dpASP.

4.2 Programming Interface Timings

The digital interface consists of a simple 3 pin SPI interface – SCK, SDI and SSb. The 16 bit control word is entered as 2 serial bytes, as shown in figure 5. The timings for this interface are shown in table 2.

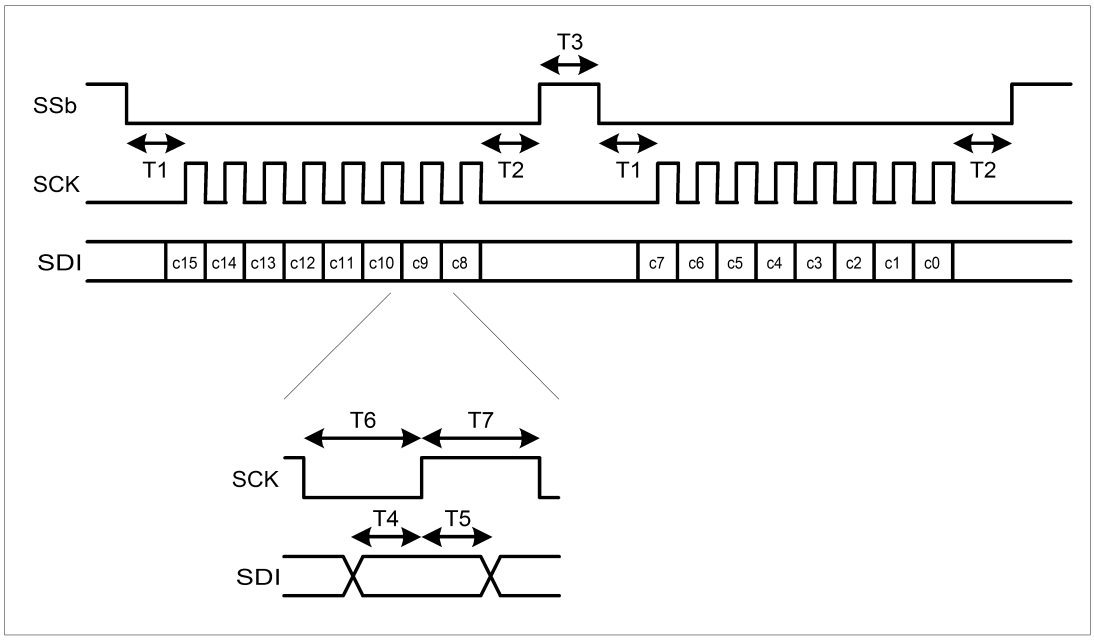

Figure 5: The Control Word

Symbol	Description	Min	units
T1	SSb falling to SCK rising	500	ns
T2	SSb rising after SCK falling	790	ns
T3	SSb high period	6.5	us
T4	SDI setup to SCK rising	100	ns
T5	SDI hold after SCK rising	100	ns
T6	SCK low period	520	ns
T7	SCK high period	520	ns

Table 2: Control Word timings

Document revision 1.0.3, 3rd April 2006
Author: Dave Lovell
Doc No. AP0238K2-U001a

4.3 Control Word

The meaning of each bit in the 16 bit control word is shown in table 3.

This is the control word for the AN238C04, state machine

ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)															
Select circuit		**Notch filter center frequency**		**Gain control**				**Lower subcarrier frequency (this sets lower bandpass or Highpass filter)**				**Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)**			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														**LSB**
A1	**A2**	**A3**	**A4**	**G1**	**G2**	**G3**	**G4**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
A1A2, 11 = Tripleband filter *(Note 3)*	**A1A2, 00 = Universal (WIDE) bandpass** A1A2, 01 = EPCGen2 (TWIN) filter A1A2, 10 = "Class0" bandpass *(see Note2)*	B1,B2	Freq (kHz)	G1,G2, G3,G4	Bulk Gain (dB)	LF gain (dB) (Note6)	HF gain (dB) (Note7)	LF1,LF2, LF3,LF4		Freq (KHz)		HF1,HF2, HF3.HF4		Freq (KHz)	
		00	*Note4*	0000	*Note5*	*Note5*	*Note5*	0000		2		0000		4	
		01	**50.0**	**0001**	**0**	+0	+0	0001		4		0001		8	
		10	52.0	0010	+6	+0	+0	0010		8		0010		16	
		11	54.0	0011	+12	+0	+0	0011		16		0011		20	
				0100	+18	+0	+0	0100		20		0100		32	
				0101	+24	+0	+0	0101		32		0101		40	
				0110	+30	+0	+0	**0110**		**40**		0110		64	
				0111		Not used		0111		64		0111		80	
				1000	+0	+3	+0	1000		80		1000		106	
				1001	+0	+6	+0	1001		106		1001		128	
				1010	+0	+12	+0	1010		128		1010		160	
				1011		Not used		1011		160		1011		212	
				1100	+0	+0	+3d	1100		212		1100		256	
				1101	+0	+0	+6	1101		256		**1101**		**320**	
				1110	+0	+0	+12	1110		320		1110		640	
				1111		Not used		1111		424		1111		848	

Table 3: 16 bit control word

Notes
1) bold - Bold text indicates the default circuit, the RangeMaster chipset will start-up with this circuit
2)"Class0", 2.2/3.3MHz Gain = 0dB. No bulk gain or balance control – the default circuit has HF and LF gain boost of +12dB.
circuit has HF & LF gain boost of +12dB. Total HF gain of x10 (20dB) and LF gain of x4 (12dB), therefore these can only be lowered.
3) lowest filter corner frequency is always one third of the highest frequency, the summing stage input branch gain=+6db Fixed
4) The notch filter is removed from the signal path. Notch filter is only used in the Universal WIDE filter
5) Control word 0000000000000000(binary), 0x00, 0x00 (Hex) sets the chipset into standby (low power mode)
6) Nominal gain = 0dB. higher gain for Lower bandpass v.s. higher bandpass
7) Nominal gain = 0dB. higher gain for higher bandpass v.s. lower bandpass
8) The anti-saturation control is via a hardware pin only
9) The "Auto-nulling" of all FPAA OpAmps shall be performed at each full reset/power-up cycle.