



AN220E04 Datasheet

Dynamically Reconfigurable FPAA



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AN220E04 Datasheet – Dynamically Reconfigurable FPAA

PRODUCT AND ARCHITECTURE OVERVIEW

The AN220E04 is the first member of Anadigm®'s second generation FPAA family – the Anadigmvortex family. Based on a fully differential switched-capacitor architecture, this new product family features higher bandwidth, improved total harmonic distortion (THD) and the ability to implement a host of advanced functions.

The AN220E04 consists of a 2 x 2 matrix of fully configurable switched capacitor configurable analog blocks (CABs), enmeshed in a fabric of programmable interconnect resources. These programmable features are directed by an on-chip SRAM configuration memory. The four CABs have access to a single Look-Up Table (LUT) which can be used to implement non linear functions such as user-defined input-to-output transfer functions, and arbitrary signal waveform generation.

Analog input signals come in from the outside world via the four input cells. The fourth input cell of the AN220E04 has a special 'multiplexing' feature which allows the connection of up to four unique signal sources. An input cell can accept either a single-ended signal or a differential signal pair. The input cells each have built-in programmable anti-aliasing filters, as well as a high gain amplifier which has an optional chopper stabilized operating mode designed for use with signals requiring significant gain and hence ultra low input offset voltages.

The AN220E04 is also designed to support dynamic reconfiguration. There are two memories on the AN220E04:

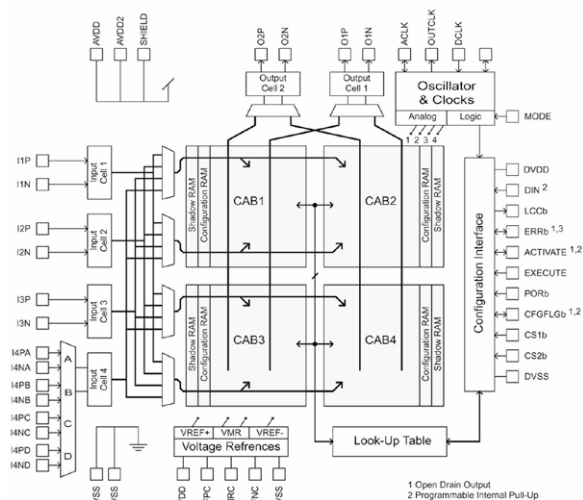


Figure 1: Architectural overview of the AN220E04 device

Shadow SRAM and Configuration SRAM. The new reconfiguration data is stored in the Shadow SRAM, which can then be transferred to the Configuration SRAM at just a single clock edge providing for synchronized on-the-fly update of the analog circuit function.

PRODUCT FEATURES

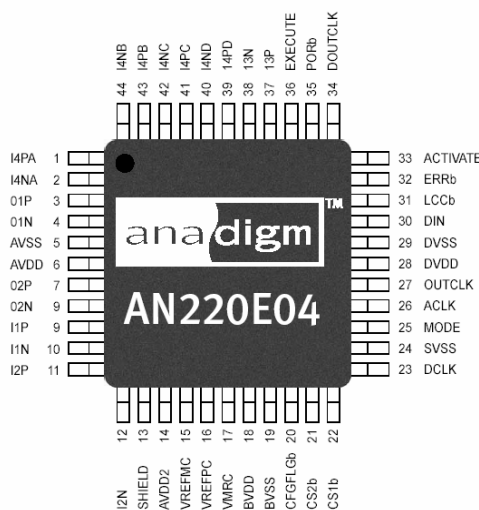
- **Dynamic reconfiguration**
- Fully differential architecture
- Fully differential I/O buffering with options for single ended to differential conversion
- Low input offset through chopper stabilized amplifiers
- Built-in Successive Approximation Register (SAR)
- 256 Byte Look-Up Table (LUT) for linearization and arbitrary signal generation
- 4:1 Input multiplexer
- Typical Signal Bandwidth: DC-2MHz (Bandwidth is CAM dependent)
- Signal to Noise Ratio:
 - Broadband 80dB
 - Narrowband (audio) 100dB
- Total Harmonic Distortion (THD): 80dB
- DC offset <100µV
- Package: 44-pin QFP
 - Lead pitch 0.8mm
- Supply voltage: 5V

ORDERING CODES

| | |
|----------------|--|
| AN220E04-QFSP | Dynamically reconfigurable FPAA Sample Pack |
| AN220E04-QFPTY | Dynamically reconfigurable FPAA Tray (96 pcs) |
| AN220E04-QFPTR | Dynamically reconfigurable FPAA Tape & Reel (1000 pcs) |
| AN220D04-EVAL | AN220E04 Evaluation Kit |
| AN220D04-DEVLP | AN220E04 Development Kit |

APPLICATIONS

- Real-time software control of analog system peripherals
- Intelligent sensors
- Adaptive filtering and control
- Adaptive DSP front-end
- Adaptive industrial control and automation
- Self-calibrating systems
- Compensation for aging of system components
- Dynamic recalibration of remote systems
- Ultra-low frequency signal conditioning
- Custom analog signal processing



[For more detailed information on the features of the AN220E04 device, please refer to the AN120E04/AN220E04 User Manual]

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------------------|-------------------------|---------|-----|-------------|------|--|
| DC Power Supplies | AVDD(2) BVDD DVDD | -0.5 | - | 5.5 V | V | AVSS, BVSS, DVSS and SVSS all held to 0.0 V ^a |
| xVDD to xVDD Offset | | -0.5 | | 0.5 | V | Ideally all supplies should be at the same voltage |
| Package Power Dissipation | Pmax 25°C Pmax 85°C | - | - | 1.8 0.73 | W | Still air, No heatsink, 4 layer board, 44 pins. $\theta_{ja} = 55^{\circ}\text{C/W}$ |
| Analog and Digital Input Voltage | Vinmax | Vss-0.5 | - | Vdd+0.5 | V | |
| Ambient Operating Temperature | Top | -40 | - | 85 | °C | |
| Storage Temperature | Tstg | -65 | | 150 | °C | |

^a Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for Vdd of up to 7 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-----------------------|-------------------------|---------|------|---------|------|--|
| DC Power Supplies | AVDD(2) BVDD DVDD | 4.75 | 5.00 | 5.25 | V | AVSS, BVSS, DVSS and SVSS all held to 0 V |
| Analog Input Voltage. | Vina | VMR-1.9 | - | VMR+1.9 | V | VMR is 2.0 volts above AVSS |
| Digital Input Voltage | Vind | 0 | - | DVDD | V | |
| Junction Temp | Tj | -40 | - | 125 | °C | Assume a package $\theta_{ja} = 55^{\circ}\text{C/W}$ ^b |

^b In order to calculate the junction temperature you must first empirically determine the current draw (total Idd) for the design. Once the current consumption established then the following formula can be used; $T_j = T_a + I_{dd} \times V_{dd} \times 55^{\circ}\text{C/W}$, where T_a is the ambient temperature. The worst case θ_{ja} of 55 °C/W assumes no air flow and no additional heatsink of any type.

General Digital I/O Characteristics (Vdd = 5v +/- 10%, -40 to 85 deg.C)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-----------------------|--------|-----|-------|------|------|---|
| Input Voltage Low | Vih | 0 | - | 30 | - | % of DVDD |
| Input Voltage High | Vil | 70 | - | 100 | - | % of DVDD |
| Output Voltage Low | Vol | 0 | - | 20 | - | % of DVDD |
| Output Voltage High | Voh | 80 | - | 100 | - | % of DVDD |
| Input Leakage Current | Iil | - | - | ±1.0 | µA | All pins except DCLK |
| Input Leakage Current | Iil | - | ±12.0 | - | µA | DCLK if a crystal is connected and the on-chip oscillator is used |
| Max. Capacitive Load | Cmax | - | - | 10 | pF | The maximum load for a digital output is 10 pF // 10 Kohm |
| Min. Resistive Load | Rmin | 10 | - | - | Kohm | The maximum load for a digital output is 10 pF // 10 Kohm |
| DCLK Frequency | Fmax | - | - | 40 | MHz | For MODE = 1, Max DCLK is 16 MHz |
| ACLK Frequency | Fmax | - | - | 40 | MHz | Divide down to <8 MHz prior to use as a CAB clock |
| Clock Duty Cycle | - | 45 | - | 55 | % | All clocks |

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Detailed Digital I/O Interface Characteristics: Vdd = 5.0volts

LCCb

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------|---------------------|-----------------|-----|-----------------|------|--------------------------------------|
| Output Voltage Low | V _{ol} | V _{ss} | - | 150 | mV | Load 20pF//50Kohm to V _{ss} |
| Output Voltage High | V _{oh} | 4.5 | - | V _{dd} | V | Load 20pF//50Kohm to V _{ss} |
| Max. Capacitive Load | C _{max} | - | - | 20 | pF | Maximum load 20 pF // 50 Kohm |
| Min. Resistive Load | R _{min} | 50 | - | - | Kohm | Maximum load 20 pF // 50 Kohm |
| Current Sink | I _{snkmax} | - | - | 15 | mA | LCCb pin shorted to V _{dd} |
| Current Source | I _{srcmax} | - | - | 4 | mA | LCCb pin shorted to V _{ss} |

CFGFLG, ACTIVATE

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---------------------------|------------------------|-----------------|-----|-----------------|------|--|
| Input Voltage Low | V _{il} | 0 | | 30 | % | % of DVDD |
| Input Voltage High | V _{ih} | 70 | | 100 | % | % of DVDD |
| Output Voltage Low | V _{ol} | V _{ss} | - | 85 | mV | Pin load = Internal pullup + 20pF//50K to V _{ss} |
| Output Voltage High | V _{oh} | 4.5 | - | V _{dd} | V | Pin load = Internal pullup + 20pF//50K to V _{ss} |
| Output Voltage Low | V _{ol} | V _{ss} | - | 200 | mV | Pin Load = External 5K ohm pullup + 20pF//50K to V _{ss} |
| Output Voltage High | V _{oh} | 4.5 | - | V _{dd} | V | Pin Load = External 5Kohm pullup + 20pF//50K to V _{ss} |
| Max. Capacitive Load | C _{max} | - | - | 50 | pF | Maximum load 50 pF // 50 Kohm |
| Min. Resistive Load | R _{min} | 50 | - | - | Kohm | Maximum load 50 pF // 50 Kohm |
| Current Sink | I _{snkmax} | - | - | 2.5 | mA | Pin shorted to V _{dd} |
| Current Source | I _{srcmax} | - | - | 200 | μA | Pin shorted to V _{ss} |
| External Resistive Pullup | R _{pullupext} | 5 | 7.5 | 10 | Kohm | Use only if internal pullup is deselected |

ERRb

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---------------------------|------------------------|-----------------|-----|-----------------|------|-------------------------------|
| Input Voltage Low | V _{il} | 0 | | 30 | % | % of DVDD |
| Input Voltage High | V _{ih} | 70 | | 100 | % | % of DVDD |
| Output Voltage Low | V _{ol} | V _{ss} | - | 50 | mV | |
| Output Voltage High | V _{oh} | 4.9 | - | V _{dd} | V | |
| Max. Capacitive Load | C _{max} | - | - | 50 | pF | Maximum load 50 pF // 50 Kohm |
| Min. Resistive Load | R _{min} | 50 | - | - | Kohm | Maximum load 50 pF // 50 Kohm |
| Current Sink | I _{snkmax} | - | - | 10 | mA | |
| Current Source | I _{srcmax} | - | - | 0 | μA | |
| External Resistive Pullup | R _{pullupext} | 10 | 10 | 10 | Kohm | |

DCLK, Mode, DIN, EXECUTE, PORb, CS1b, CS2b

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--------------------|-----------------|-----|-----|-----|------|-----------|
| Input Voltage Low | V _{il} | 0 | - | 30 | % | % of DVDD |
| Input Voltage High | V _{ih} | 70 | - | 100 | % | % of DVDD |

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OUTCLK/SPIMEM,DOUTCLK

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------|---------------------|-----|-----|-----|------|-------------------------------|
| Output Voltage Low | V _{ol} | 0 | - | 20 | % | % of DVDD |
| Output Voltage High | V _{oh} | 80 | - | 100 | % | % of DVDD |
| Max. Capacitive Load | C _{max} | - | - | 50 | pF | Maximum load 50 pF // 50 Kohm |
| Min. Resistive Load | R _{min} | 10 | - | - | Kohm | Maximum load 50 pF // 50 Kohm |
| Current Sink | I _{snkmax} | - | - | 17 | mA | |
| Current Source | I _{srcmax} | - | - | 4 | mA | |

ACLK/SPIP

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------|---------------------|-----|-----|-----|------|-------------------------------|
| Input Voltage Low | V _{il} | 0 | - | 30 | % | % of DVDD |
| Input Voltage High | V _{ih} | 70 | - | 100 | % | % of DVDD |
| Output Voltage Low | V _{ol} | 0 | - | 20 | % | % of DVDD |
| Output Voltage High | V _{oh} | 80 | - | 100 | % | % of DVDD |
| Max. Capacitive Load | C _{max} | - | - | 50 | pF | Maximum load 50 pF // 50 Kohm |
| Min. Resistive Load | R _{min} | 10 | - | - | Kohm | Maximum load 50 pF // 50 Kohm |
| Current Sink | I _{snkmax} | - | - | 15 | mA | |
| Current Source | I _{srcmax} | - | - | 4 | mA | |

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Analog Inputs General

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|----------------------|-----|-----|--------|------|--|
| High Precision Input Range ^c | V _{ina} | 0.5 | - | 3.5 | V | VMR +/- 1.5v |
| Standard precision Input Range ^d | V _{ina} | 0.1 | - | 3.9 | V | VMR +/- 1.9v |
| High Precision Differential Input ^c | V _{diffina} | 0 | - | +/-3.0 | V | Common mode voltage = 2 V |
| Standard Precision Differential Input ^d | V _{diffina} | 0 | - | +/-3.8 | V | Common mode voltage = 2 V |
| Common Mode Input Range | V _{cm} | 1.8 | 2.0 | 2.2 | V | |
| Input Offset | V _{os} | - | 5 | 15 | mV | Non-chopper stabilized input |
| Input Frequency | F _{ain} | 0 | <2 | 8 | MHz | Max value is clock, CAM and input stage dependant. Input frequency is limited to approx <2MHz due to CAM signal processing which is based on sampled data architectures. |

^c High precision operating range provides optimal linearity and dynamic range.

^d Standard precision operating range provides maximum dynamic range and reduced linearity.

Input Differential Amplifier ON and filter OFF

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|--|------------------------|-----|-----|-----------|--|
| Input Range | V _{ina} V _{diffina} | See analog input above | | | | Usable input range will be reduced by the effective gain setting |
| Gain Setting | G _{inamp} | 16 | - | 128 | | |
| Gain Accuracy | | - | 1.0 | 2.5 | % | |
| Gain Drift (Temperature, Supply Voltage and Time) | Dist | - | - | 1.0 | % | |
| Equivalent Input Offset Voltage | V _{os} | - | 3 | 12 | mV | Non-chopper stabilized input When the input amplifier and filter are used in combination V _{os} contribution comes only from the input amplifier |
| Offset Voltage Temperature Coefficient | V _{offsettc} | - | 1 | 10 | μV/°C | from -40°C to 125°C |
| Input Frequency ^c | F _{ain} | 0 | - | 2 | MHz | |
| Input Frequency ^d | F _{ain} | 0 | <2 | 8 | MHz | |
| Power Supply Rejection Ratio | PSRR | 65 | - | - | dB | d.c. Amp Gain =16 a.c. See graphs page 18 |
| Common Mode Rejection Ratio | CMRR | - | 67 | - | dB | |
| Large Signal Harmonic Distortion | Dist | - | -65 | - | dB | 0.4v p-p Differential input at 660Hz Gain setting = 16 |
| Input Resistance | R _{in} | 10 | | - | Mohm | |
| Input Capacitance | C _{in} | - | | 5.0 | pF | |
| Input Referred Noise Figure | NF | - | 0.1 | - | μV/sqrtHz | Input cell Gain = 16 Applies to audio frequency range (400Hz to 30KHz). See graphical data on page 18 |
| Signal-to Noise Ratio and Distortion | SINAD | - | 75 | - | dB | Input signal = 285 mV p-p diff, audio frequency range See graphical data on page 18 |
| Spurious Free Dynamic Range | SFDR | - | 73 | - | dB | Input signal = 100 mV p-p diff See graphical data on page 18 |

^c High precision operating range provides optimal linearity and dynamic range.

^d Standard precision operating range provides maximum dynamic range and reduced linearity.

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Input Differential Chopper Amplifier ON and Filter OFF

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---|------------------------|---------------------|--------------------|-----------|--|
| Input Range | V _{ina} V _{difffina} | See analog input above | | | | Usable input range will be reduced by the effective gain setting |
| Gain Setting | G _{inamp} | 16 | - | 128 | | |
| Gain Accuracy | | - | 1.0 | 2.5 | % | |
| Gain Drift, (Temperature, Supply Voltage and Time) | | - | - | 1.0 | % | |
| Chopper Frequency Clock Range | F _{ch} | F _c /260100 | - | >250 | KHz | F _c = master clock frequency Set F _{ch} as slow as possible F _{ch} > 250KHz will result in some signal attenuation |
| Equivalent Input Offset Voltage | V _{os} | - | <100 | 200 | μV | Chopper stabilized amplifier The maximum value of 200μV is guaranteed by production test This is a tester limitation |
| Offset Voltage Temperature Coefficient | V _{offsettc} | - | 0.5 | 2.0 | μV/°C | from -40°C to 125°C |
| Power Supply Rejection Ratio | PSRR | 65 | - | - | dB | d.c. a.c. See graphs on page 18 |
| Common Mode Rejection Ratio | CMRR | - | 102 | - | dB | |
| Large Signal Harmonic Distortion | Dist | - | -40 | - | dB | 0.4v p-p Differential input at 660Hz Gain setting = 16 |
| Input Frequency | F _{ain} | 0 | F _{ch} /20 | F _{ch} /2 | KHz | F _{ch} =Chopper clock frequency The chopper frequency and input frequency should be chosen such that subsequent low pass filtering can remove the chopper stage frequency elements |
| Input Resistance | R _{in} | 10 | | - | Mohm | Input to filter or chopper |
| Input Capacitance | C _{in} | - | | 5.0 | pF | |
| Input Referred Noise Figure | NF | - | 0.09 | - | μV/sqrtHz | Input cell Gain = 16 Applies to Audio frequency range Chopper clock F _{ch} = 250KHz See graphical data on page 18 |
| Signal-to Noise Ratio and Distortion | SINAD | - | 75 | - | dB | Input signal = 285 mV p-p differential, Audio frequency range See graphical data on page 18 |
| Spurious Free Dynamic Range | SFDR | - | 74 | - | dB | Input signal =100 mV p-p differential See graphical data on page 18 |

Input Differential Amplifier OFF and Filter ON

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---|------------------------|-------------------|-------------------|-------|---|
| Input Range | V _{ina} V _{difffina} | See analog input above | | | | |
| Equivalent Input Offset | V _{os} | - | 8 | 32 | mV | Non-chopper stabilized input, Filter corner frequency =470KHz |
| Offset Voltage Temperature Coefficient | V _{offsettc} | - | 0.05 ^I | 1.0 ^{II} | mV/°C | from -40°C to 125°C I. measured at filter corner=470KHz II. maximum at Filter corner=76KHz |
| Input Frequency | F _{ain} | - | - | - | MHz | Input filter frequency will define the maximum frequency Input filter is recommended to be >30x higher than the max input frequency, for 80dB distortion performance |

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| | | | | | | |
|--|-------------|----|------|-----|-----------|---|
| Common Mode Rejection Ratio | CMRR | - | 60 | - | dB | |
| Power Supply Rejection Ratio | PSRR | 68 | - | - | dB | d.c. a.c. See graphical data on page 19 |
| Large Signal Harmonic Distortion | Dist | - | -82 | - | dB | 4v p-p Differential input at 660Hz Filter corner frequency 470KHz |
| Input Low Pass Filter (Anti-Alias) Corner Frequency Settings | Ffiltcorner | 76 | - | 470 | KHz | |
| Input Resistance | Rin | 10 | - | - | Mohm | Input to filter or chopper |
| Input Capacitance | Cin | - | - | 5.0 | pF | |
| Input Referred Noise Figure | NF | - | 0.17 | - | μV/sqrtHz | Input cell filter corner Fc = 470KHz Applies to Audio frequency range See graphical data on page 18 |
| Signal-To Noise Ratio and Distortion | SINAD | - | 84 | - | dB | Input signal = 1400 mV p-p diff, Audio frequency range See graphical data on page 18 |
| Spurious Free Dynamic Range | SFDR | - | 90 | - | dB | Input signal =1400 mV p-p differential See graphical data on page 18 |

Input Differential Voltage mode, Amplifier OFF, Filter OFF and Unity Gain Stage ON

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|------------------|------------------------|------|-----|-----------|--|
| Input Range | Vina Vdiffina | See analog input above | | | V | |
| Equivalent Input Offset | Vos | - | 5 | 15 | mV | Non-chopper stabilized input |
| Offset Voltage Temperature Coefficient | Voffsettc | - | 20 | 50 | μV/°C | from -40°C to 125°C |
| Input Frequency | Fain | - | - | 1.0 | MHz | Gain Bandwidth limited by input impedance |
| Power Supply Rejection Ratio | PSRR | 60 | - | - | dB | d.c. a.c. See graphs on page 18 |
| Common Mode Rejection Ratio | CMRR | - | 60 | - | dB | |
| Large Signal Harmonic Distortion | Dist | - | -80 | - | dB | 4v p-p Differential input at 660Hz |
| Large Signal Harmonic Distortion | Dist | - | -80 | - | dB | 3v p-p single ended signal at 660Hz |
| Input Resistance | Rin | - | 126 | - | Kohm | Input to unity gain stage |
| Input Capacitance | Cin | - | 2.0 | 5.0 | pF | |
| Input Referred Noise Figure | NF | - | 0.16 | - | μV/sqrtHz | Applies to Audio frequency range See graphical data on page 18 |
| Signal-To Noise Ratio and Distortion | SINAD | - | 84 | - | dB | Input signal = 1400 mV p-p diff, Audio frequency range See graphical data on page 18 |
| Spurious Free Dynamic Range | SFDR | - | 90 | - | dB | Input signal =1400 mV p-p differential See graphical data on page 18 |

Input Differential Voltage mode, Amplifier OFF, Filter OFF and Unity Gain stage OFF

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|------------------|------------------------|-----|-----|-------|---|
| Input Range | Vina Vdiffina | See analog input above | | | V | |
| Equivalent Input Offset | Vos | N/A | N/A | N/A | mV | See CAM Op Amp |
| Offset Voltage Temperature Coefficient | Voffsettc | N/A | N/A | N/A | μV/°C | See CAM Op Amp. from -40°C to 125°C |
| Input Frequency | Fain | - | - | 8 | MHz | Dependant upon CAM |
| Power Supply Rejection Ratio | PSRR | N/A | N/A | N/A | dB | See CAM Op Amp |
| Large Signal Harmonic Distortion | Dist | - | -85 | - | dB | See CAM Op Amp |
| Input Resistance | Rin | - | - | - | Mohm | Input to CAM directly (Input cell bypass mode). This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture |
| Input Capacitance | Cin | - | - | - | pF | Input to CAM directly (Input cell bypass mode) This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture |

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Analog Outputs

(See "Output Cell" section in the AN120E04/AN220E04 user manual for more details)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------|-----|-----|--------|------|---------------------------|
| High Precision Output Range ^c | Vouta | 0.5 | - | 3.5 | V | VMR +/- 1.5v |
| Standard Precision Output Range ^d | Vouta | 0.1 | - | 3.9 | V | VMR +/- 1.9v |
| High Precision Differential Output ^c | Vdiffouta | - | - | +/-3.0 | V | Common mode voltage = 2 V |
| Standard precision Differential Output ^d | Vdiffouta | - | - | +/-3.8 | V | Common mode voltage = 2 V |
| Common Mode Voltage | Vcm | 1.9 | 2.0 | 2.1 | V | |

^c. High precision operating range provides optimal linearity and dynamic range.

^d. Standard precision operating range provides maximum dynamic range and reduced linearity.

Output Voltage mode and filter ON, corner frequency 470KHz

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|------------------|------------------------|-------------------|-------------------|-----------|--|
| Input Range | Vina Vdiffina | See analog input above | | | V | |
| Equivalent Input Offset | Vos | - | 5 | 15 | mV | |
| Offset Voltage Temperature Coefficient | Voffsetc | | 0.05 ⁱ | 1.0 ⁱⁱ | mV/°C | from -40°C to 125°C ⁱ measured at filter corner: 470KHz ⁱⁱ maximum at filter corner: 76KHz |
| Output Frequency | Faout | - | - | - | MHz | Output filter frequency will define the maximum frequency Input filter is recommended to be >30x higher than the max input frequency, for good distortion performance |
| Power Supply Rejection Ratio | PSRR | 60 | - | - | dB | d.c. a.c. See graphical data on page 19 |
| Large Signal Harmonic Distortion | Dist | - | -82 | - | dB | 4v p-p Differential input at 660Hz Filter corner frequency 470KHz |
| Input Low Pass Filter (Anti-Alias) Corner Frequency Settings | Ffiltcorner | 76 | - | 470 | KHz | |
| Output Load ^{c,e} | Rload | 0.1 | - | - | Mohm | |
| Output Load ^{c,e} | Cload | - | - | 50 | pF | |
| Output Load ^{d,e} | Rload | 1 | 10 | - | Kohm | Additional loading causes internal voltage drops across output stage and series resistances The output stage has a small signal output impedance of approx 10ohm |
| Output Load ^{d,e} | Cload | - | - | 100 | pF | |
| Common Mode Rejection Ratio | CMRR | - | 56 | - | dB | |
| Input Referred Noise Figure | NF | - | 0.22 | - | µV/sqrtHz | Output filter corner fc = 470KHz Applies to Audio frequency range See graphical data on page 18 |
| Signal-To Noise Ratio and Distortion | SINAD | - | 82 | - | dB | Input signal = 1400 mV p-p diff, Audio frequency range See graphical data on page 18 |
| Spurious Free Dynamic Range | SFDR | - | 90 | - | dB | Input signal =1400 mV p-p diff See graphical data on page 18 |

^c. High precision operating range provides optimal linearity and dynamic range.

^d. Standard precision operating range provides maximum dynamic range and reduced linearity.

^e. The maximum load for an analog output is 50 pF // 100 Kohms. This load maybe with respect to analog ground VMR or AVSS.

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Output Voltage mode and filter off (bypass mode)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---|------------------------|-----|-----|-------|---|
| Input Range | V _{ina} V _{difffina} | See analog input above | | | V | |
| Equivalent Input Offset | V _{os} | N/A | N/A | N/A | mV | See CAM Op Amp |
| Offset Voltage Temperature Coefficient | V _{offsettc} | N/A | N/A | N/A | mV/°C | See CAM Op Amp |
| Output Frequency ^{c,e} | F _{out} | - | - | 4 | MHz | |
| Output Frequency ^{d,f} | F _{out} | - | - | 8 | MHz | The realizable output frequency is limited to approx <2MHz due to CAM signal processing which is based on sampled data architectures. |
| Power Supply Rejection Ratio | PSRR | N/A | N/A | N/A | dB | See CAM Op Amp |
| Large Signal Harmonic Distortion | Dist | - | -85 | - | dB | |
| Output Load | R _{load} | N/A | N/A | N/A | Mohm | See CAM Op Amp |
| Output Load | C _{load} | N/A | N/A | N/A | pF | See CAM Op Amp |

^c. High precision operating range provides optimal linearity and dynamic range.

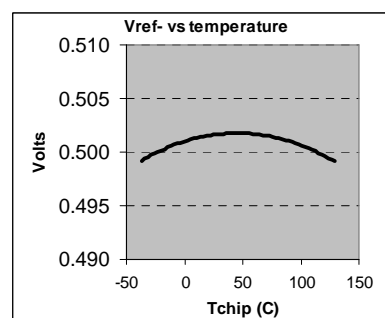
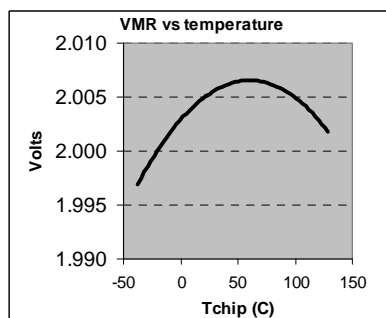
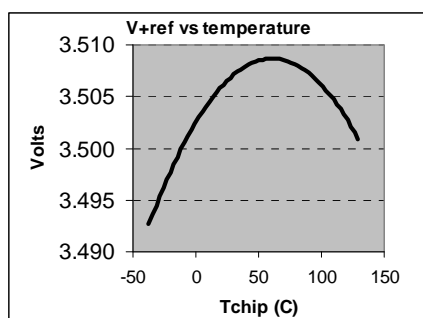
^d. Standard precision operating range provides maximum dynamic range and reduced linearity.

^e. The maximum load for an analog output is 50 pF // 100 Kohms. This load maybe with respect to analog ground VMR or AVSS.

^f. The maximum load for an analog output is 100 pF // 100 Kohms. This load must be differential and with respect to analog ground(VMR).

VMR (voltage Mid Rail) and VREF (Reference Voltage) Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|---------------------|-------|-------|-------|------|---|
| VMR Output Voltage | V _{vmr} | 1.925 | 2.01 | 2.075 | V | At 25°C, V _{dd} =5.00 volts |
| VREF+ Output Voltage | V _{ref+} | 3.4 | 3.51 | 3.6 | V | At 25°C, V _{dd} =5.00 volts |
| VREF- Output Voltage | V _{ref-} | 0.45 | 0.505 | 0.55 | V | At 25°C, V _{dd} =5.00 volts |
| Output Voltage Deviation VREF+, VMR, VREF- | V _{refout} | - | 0.5 | 1 | % | Over process and supply voltage corners |
| Voltage Temperature Coefficient VREF+, VMR, VREF- | V _{reftc} | - | - | - | - | See typical graphical data below -40°C to 125°C ^f |
| Power Supply Rejection Ratio, VMR | PSSR | 60 | - | - | dB | |
| Power Supply Rejection Ratio V _{ref+} and V _{ref-} | PSSR | 75 | - | - | dB | |
| Start Up Time | T _{start} | - | - | 1 | ms | Assuming recommended capacitors |



AN220E04 Datasheet – Dynamically Reconfigurable FPAA

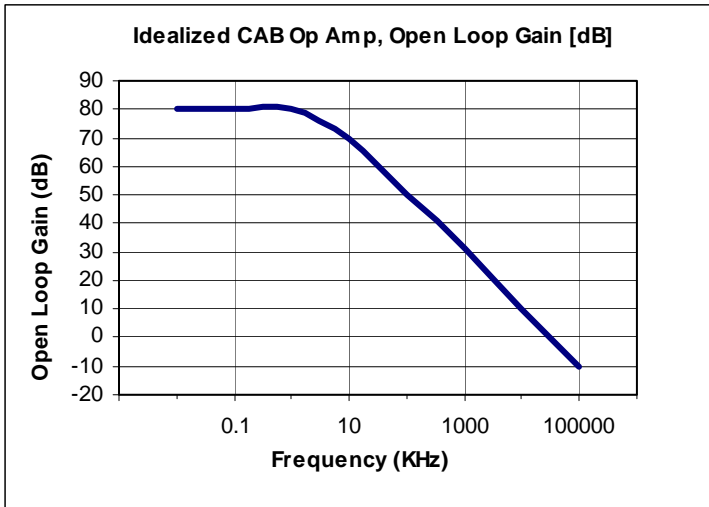
CAB (Configurable Analog Block) Differential Operational Amplifier

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------|-----|------|--------|-----------|--|
| High Precision Input/Output Range ^c | Vinouta | 0.5 | - | 3.5 | V | VMR +/- 1.5v |
| Standard Precision Input/Output Range ^d | Vinouta | 0.1 | - | 3.9 | V | VMR +/-1.9v |
| High Precision. Differential Input/Output ^c | Vdiffioa | - | - | +/-3.0 | V | Common mode voltage = 2 V |
| Standard Precision Differential Input/Output ^d | Vdiffioa | - | - | +/-3.8 | V | Common mode voltage = 2 V |
| Common Mode Input Voltage Range ^d | Vcm | 0 | 2.0 | 4 | V | |
| Common Mode Output Voltage Range | Vcm | 1.9 | 2.0 | 2.1 | V | |
| Equivalent Input Voltage Offset. | Voffset | 0.1 | 5 | 15 | mV | Some CAMs (Configurable Analog Modules) can inherently compensate |
| Offset Voltage Temperature Coefficient | Voffsettc | - | 1 | 10 | μV/°C | from -40°C to 125°C some CAMs (Configurable Analog Modules) can inherently compensate |
| Power Supply Rejection Ratio | PSSR | - | 80 | - | dB | Variation between CAMs is expected because of variations in architecture |
| Common Mode Rejection Ratio | CMRR | - | 77 | - | dB | Example 1 GainInv CAM CAM clock = 1MHz CAM parameter settings Gain = 1 |
| Common Mode Rejection Ratio | CMRR | - | 60 | - | dB | Example 2 Filterbiquad Setting = Low pass filter CAM clock = 1MHz CAM parameter settings Gain = 1, Corner frequency = 50KHz Quality Factor = 0.707 |
| Differential Slew Rate, Internal | Slew | - | 50 | - | V/μsec | Applicable when the OpAmp load is internal to the FPAA |
| Differential Slew Rate, External | Slew | - | 10 | - | V/μsec | Applicable when the OpAmp driving signal out of the FPAA package |
| Unity Gain Bandwidth, Full Power Mode. | UGB | - | 50 | - | MHz | Applicable when sourcing and loading the OpAmp with a load internal to the FPAA |
| Input Impedance, Internal | Rin | 10 | - | - | Mohm | |
| Output Impedance, Internal | Rout | - | - | - | Ohms | The OpAmp output is designed to drive all internal nodes, these are dominantly capacitive loads |
| Output Impedance, External | Rout | - | - | - | Ohms | Output to an FPAA output pin (output cell bypass mode). This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture |
| Output Load, External ^{c e} | Rload | 0.1 | - | - | Mohm | |
| Output Load, External ^{c e} | Cload | - | - | 50 | pF | |
| Output Load, External ^{d e f} | Rload | 1 | 10 | - | Kohm | Additional loading causes internal voltage drops across output stage and series resistances The output stage has a small signal output impedance of approx 10ohm |
| Output Load, External ^{d e f} | Cload | - | - | 50 | pF | |
| Noise Figure ^g | Noise | - | 0.13 | - | μV/sqrtHz | Example1 GainInv CAM CAM clock = 1MHz Gain = 1 |

AN220E04 Datasheet – Dynamically Reconfigurable FPAA

| | | | | | | |
|---|-------|---|----|---|----|--|
| Signal-To Noise Ratio and Distortion ^g | SINAD | - | 80 | - | dB | Input signal=1400 mV p-p differential Audio frequency range Example. GainInv CAM CAM clock = 1MHz Gain = 1 |
| Spurious Free Dynamic Range ^g | SFDR | - | 92 | - | dB | Input signal=1400 mV p-p differential, Audio frequency range Example. GainInv CAM CAM clock = 1MHz Gain = 1 |

- ^c. High precision operating range provides optimal linearity and dynamic range.
- ^d. Standard precision operating range provides maximum dynamic range and reduced linearity.
- ^e. The maximum load for an analog output is 50 pF || 100 Kohms. This load may be with respect to analog ground VMR or AVSS.
- ^f. Using the FPAA with CAB Op Amp's driving directly off-chip, requires care, full characterization of the performance of each application circuit by the circuit designer is necessary.
- ^g. This specification parameter can only be characterized when a circuit topology is configured onto the CAB differential amplifier architecture. The figure provided here is an representative on the performance of one specific CAM, as specified in the comments.



The idealized open loop gain plot is provided for information only. This information is associated with the FPAA in full power mode of operation. The FPAA operation amplifier open loop gain cannot be observed nor used when associated with external connections to the device. Internal reprogrammable routing impedances and switched capacitor circuit architecture using this operational amplifier limit the effective usable bandwidth of a circuit realized in the FPAA to less than 2MHz.

AN220E04 Datasheet – Dynamically Reconfigurable FPAA

CAB (Configurable Analog Block) Differential Comparator

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------------|---------------------|----------------------|----------------------|-------|--|
| Input Range, Internal | V _{ina} | 0.1 | - | 3.9 | V | |
| Input Range, External | V _{ina} | 0.0 | - | V _{dd} | V | |
| Differential Input, Internal | V _{diffina} | - | - | +/-3.8 | V | Common mode voltage = 2 V |
| Differential Input, External | V _{diffina} | +/- 0.0 | - | +/- V _{dd} | V | |
| Common Mode Output Voltage Range, Internal ^c | V _{cm} | 1.9 | 2.0 | 2.1 | V | |
| Common Mode Input Voltage Range, External ^c | V _{cm} | 0 | 2.0 | 4 | V | |
| Common Mode Input Voltage, External ^d | V _{cm} | 0 | - | 5 | V | The comparator will function correctly |
| Differential Output | V _{outdiff} | - | - | +/-5 | V | |
| Single Pin Output (Ox1P) | V _{out} | 0 | - | 5 | V | |
| Input Voltage Offset | V _{offcomp} | - | 2 | 10 | mV | Zero hysteresis |
| Offset Voltage Temperature Coefficient | V _{offsettc} | - | 1 | 10 | μV/°C | from -40°C to 125°C, Zero Hysteresis |
| Setup Time, Internal | T _{setint} | - | - | 125 | nsec | |
| Setup Time, External | T _{setext} | - | - | 500 | nsec | |
| Delay Time | T _{delay} | ½T _d +25 | - | 1½T _d +25 | nsec | T _d = 1/F _c F _c = master clock frequency |
| Output Load | R _{load} | 10 | - | - | Kohm | Applies if comparator drive off chip with output cell in bypass mode |
| Output Load | C _{load} | - | - | 50 | pF | Applies if comparator drive off chip with output cell in bypass mode |
| Differential Variable Reference Voltage Settings | CompV _{ref} | 0 | - | +/-4.0 | V | |
| Differential Hysteresis | Hysta1 | - | V _{offcomp} | - | mV | Hysteresis setting = zero |
| Differential Hysteresis | Hysta2 | - | 20 | - | mV | Hysteresis setting = 10mV |
| Differential Hysteresis | Hysta3 | - | 40 | - | mV | Hysteresis setting = 20mV |
| Differential Hysteresis | Hysta4 | - | 80 | - | mV | Hysteresis setting = 40mV |
| Hysteresis Setting Accuracy | Hystb | - | 25 | - | % | |
| Hysteresis Temperature Coefficient | Hysttc1 | - | 5 | - | μV/°C | Hysteresis setting = zero |
| Hysteresis Temperature Coefficient | Hysttc2 | - | 50 | - | μV/°C | Hysteresis setting = 10mV |
| Hysteresis Temperature Coefficient | Hysttc3 | - | 100 | - | μV/°C | Hysteresis setting = 20mV |
| Hysteresis Temperature Coefficient | Hysttc4 | - | 200 | - | μV/°C | Hysteresis setting = 40mV |

^c. High precision operating range provides optimal linearity and dynamic range.

^d. Standard precision operating range provides maximum dynamic range and reduced linearity.

AN220E04 Datasheet – Dynamically Reconfigurable FPAA

ESD Characteristics

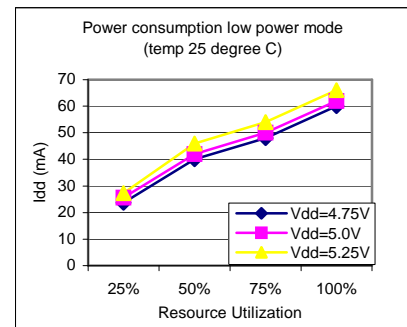
| Pin Type | Human Body Model | Machine Model | Charged Device Model |
|-----------------------|------------------|---------------|----------------------|
| Digital Inputs | 4000V | 250V | 4kV |
| Digital Outputs | 4000V | 250V | 4kV |
| Digital Bidirectional | 4000V | 250V | 4kV |
| Digital Open Drain | 4000V | 250V | 4kV |
| Analog Inputs | 2000V | 200V | 4kV |
| Analog Outputs | 1500V | 100V | 4kV |
| Reference Voltages | 1500V | 100V | 4kV |

The AN220E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN220E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Power Consumption – Low Power Mode

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---------------------------------|-----------------|-----|-----|-----|-------|---|
| Minimum Power ^{1a} | I _{dd} | - | 0.2 | - | mA | V _{dd} =5.00 volts, T _j =25°C |
| Nominal 25% Power ^{1b} | I _{dd} | - | 25 | 30 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Nominal 50% Power ^{1c} | I _{dd} | - | 42 | 47 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Nominal 75% Power ^{1d} | I _{dd} | - | 50 | 55 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Maximum Power ^{1e} | I _{dd} | - | 60 | - | mA | V _{dd} =4.75 volts, T _j =85°C |
| | | | 63 | 68 | | V _{dd} =5.00 volts, T _j =25°C |
| | | | 66 | - | | V _{dd} =5.25 volts, T _j = -40°C |
| Temperature Coefficient | - | - | -2 | -10 | µA/°C | |

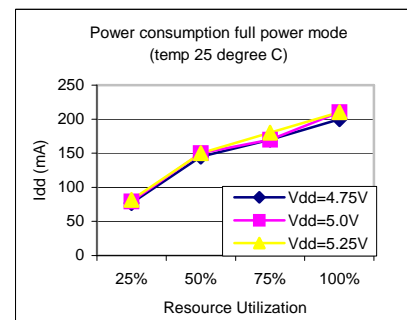
- 1a. External clock, all analog function disabled, memory active.
- 1b. FPAA active elements – Two core op-amps (low power mode), one comparator, one input (bypass mode), one output filter and differential to single-ended converter (low power mode).
- 1c. FPAA active elements – Four core op-amps (low power mode), two comparators (one using SAR), two inputs (bypass mode), two output filters and two differential to single-ended converters (low power mode).
- 1d. FPAA active elements – Six core op-amps (low power mode), three comparators (two using SAR), three inputs (bypass mode), two output filters and two differential to single-ended converters (low power mode).
- 1e. FPAA active elements – Eight core op-amps (low power mode), four comparators (two using SAR), four inputs (bypass mode), two output filters and two differential to single-ended converters (low power mode).



Power Consumption – Full Power Mode

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------|-----|-----|-----|------|---|
| Full Power Mode Minimum Power ^{2a} | I _{dd} | - | 1.5 | - | mA | V _{dd} =5.00 volts, T _j =25°C |
| Full Power Mode Nominal 25% Power ^{2b} | I _{dd} | - | 80 | 90 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Full Power Mode Nominal 50% Power ^{2c} | I _{dd} | - | 150 | 160 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Full Power Mode Nominal 75% Power ^{2d} | I _{dd} | - | 170 | 190 | mA | V _{dd} =5.00 volts, T _j =25°C |
| Full Power Mode Maximum Power ^{2e} | I _{dd} | - | 200 | - | mA | V _{dd} =4.75 volts, T _j =85°C |
| | | | 210 | 230 | | V _{dd} =5.00 volts, T _j =25°C |
| | | | 220 | - | | V _{dd} =5.25 volts, T _j = -40°C |

- 2a. AN220E04 Crystal Oscillator, all analog functions disabled, memory active.
- 2b. FPAA active elements – Two core op-amps, one comparator, one input filter and chopper amplifier, one output filter and differential to single-ended converter.
- 2c. FPAA active elements – Four core op-amps, two comparators (one using SAR), two Input filters and two chopper amplifiers, two output filters and two differential to single-ended converters.
- 2d. FPAA active elements – Six core op-amps, three comparators (two using SAR), three input filters and three chopper amplifiers, two output filters and two differential to single-ended converters.
- 2e. FPAA active elements – Eight core op-amps, four comparators (two using SAR), four input filters and two chopper amplifiers, two output filters and two differential to single-ended converters.



AN220E04 Datasheet – Dynamically Reconfigurable FPA

PINOUT

| Pin Number | Pin Name | Pin Type | Comments |
|------------|-----------------|----------------------------|--|
| 1 | I4PA | Analog IN+ | |
| 2 | I4NA | Analog IN- | |
| 3 | O1P | Analog OUT+ | |
| 4 | O1N | Analog OUT- | |
| 5 | AVSS | Analog Vss | |
| 6 | AVDD | Analog Vdd | |
| 7 | O2P | Analog OUT | |
| 8 | O2N | Analog OUT | |
| 9 | I1P | Analog IN+ | |
| 10 | I1N | Analog IN- | |
| 11 | I2P | Analog IN+ | |
| 12 | I2N | Analog IN- | |
| 13 | SHIELD | Analog Vdd | Low noise Vdd bias for capacitor array n-wells |
| 14 | AVDD2 | Analog Vdd | Analog power |
| 15 | VREFMC | Vref | Attach filter capacitor for VREF- |
| 16 | VREFPC | Vref | Attach filter capacitor for VREF+ |
| 17 | VMRC | Vref | Attach filter capacitor for VMR (Voltage Main Reference) |
| 18 | BVDD | Analog Vdd | Analog power for bandgap Vref Generators |
| 19 | BVSS | Analog Vss | Analog ground for bandgap Vref Generators |
| 20 | CFGFLGb | Digital IN | In multi-device systems... 0, Ignore incoming data (unless currently addressed) 1, Pay attention to incoming data (watching for address) |
| | | Digital OUT | 0, Device is being configured Z, Device is not being configured (if internal pullup is selected) |
| 21 | CS2b | Digital IN | 0, Chip is selected 1, Chip is not selected |
| 22 | CS1b | Digital IN (during config) | 0, Allow configuration to proceed 1, Hold off configuration |
| | | Digital IN (after config)_ | Passes read-back data through to LCC_B pin |
| 23 | DCLK | Digital IN | |
| 24 | SVSS | Digital Vss | Digital ground - substrate tie |
| 25 | MODE | Digital IN | 0, Synchronous serial interface 1, SPI EPROM Interface |
| 26 | ACLK / SPIP | Digital IN | MODE = 0, analog clock < 40 MHz |
| | | Digital OUT | MODE = 1, SPI EPROM or serial EPROM clock |
| 27 | OUTCLK / SPIMEM | Digital OUT | During power-up, sources SPI EPROM initialization command string |
| | | Digital OUT | After power-up, sources any of the four internal analog clocks |
| 28 | DVDD | Digital Vdd | |
| 29 | DVSS | Digital Vss | |
| 30 | DIN | Digital IN | Serial configuration data input |
| 31 | LCCb | Digital OUT | 1, Local configuration is needed. Once configuration is completed, it is a registered version of CS1b or if the device is addressed for read, it serves as serial data out port |
| 32 | ERRb | Digital IN (monitored OUT) | 0, Initiate reset 1, No action |
| | | Digital OUT | 0, Error condition Z, No error condition (external pullup required) |
| 33 | ACTIVATE | Digital IN | 0, Hold off completion of configuration Rising Edge, Allow completion of configuration O.D. Output 0, device has not yet completed primary configuration Z, Device has completed primary configuration (if internal pullup is selected) |
| 34 | DOUTCLK / TEST | Digital OUT | A buffered version of DCLK. |
| | | Digital IN | (Factory reserved test input. Float if unused) |
| 35 | PORb | Digital IN | 0, Chip held in reset state Rising edge, re-initiates power on reset sequence To initiate a POR reset cycle, the minimum pulse width required on the PORb pin is 25ns. |
| 36 | EXECUTE | Digital IN | 0, No action 1, Transfer shadow RAM into configuration RAM |
| 37 | I3P | Analog IN+ | |
| 38 | I3N | Analog IN- | |
| 39 | I4PD | Analog IN+ | Analog multiplexer input signals. The multiplexer can accept 4 differential inputs or 8 single ended inputs |
| 40 | I4ND | Analog IN- | |
| 41 | I4PC | Analog IN+ | |
| 42 | I4NC | Analog IN- | |
| 43 | I4PB | Analog IN+ | |
| 44 | I4NB | Analog IN- | |

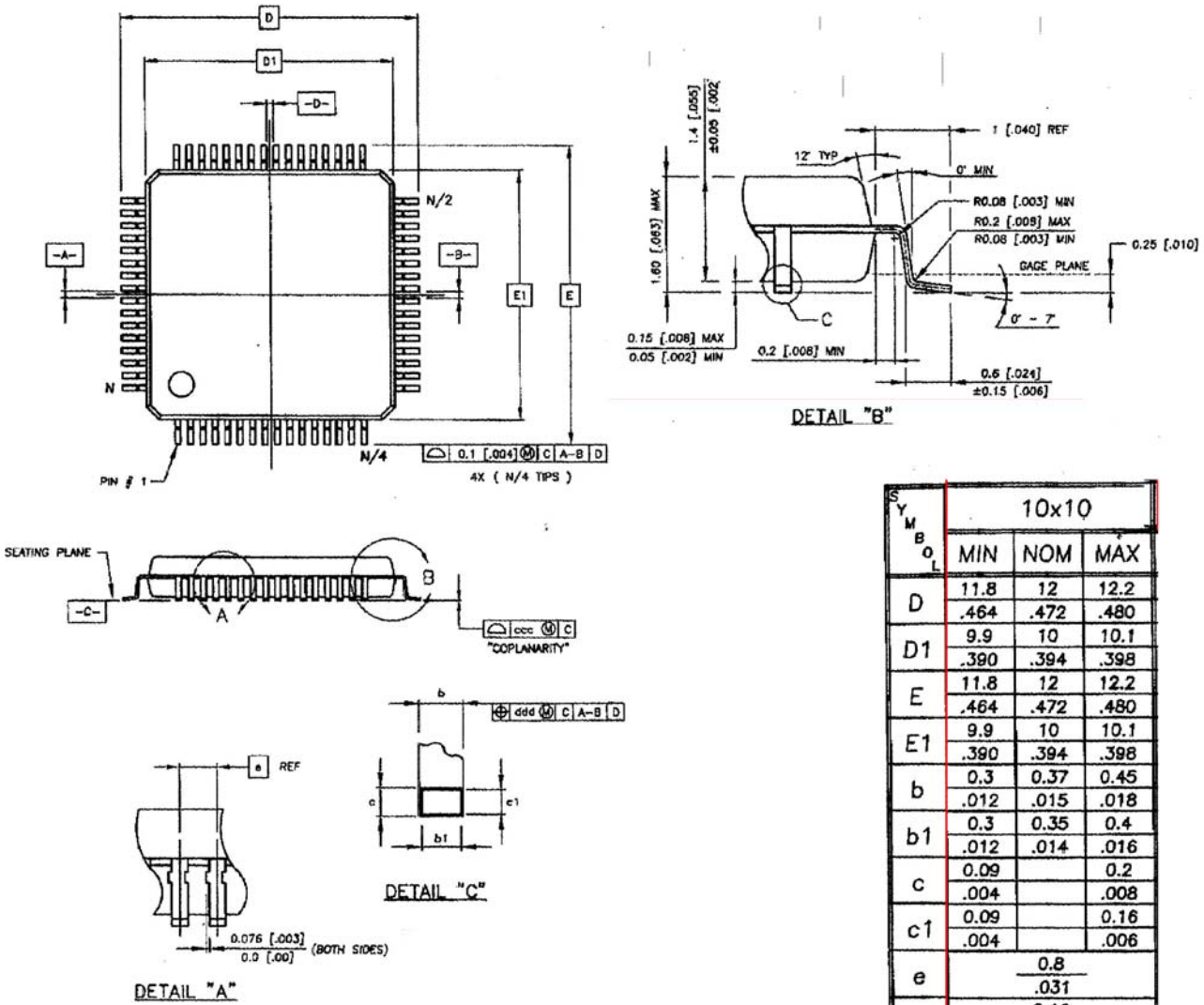
AN220E04 Datasheet – Dynamically Reconfigurable FPAA

MECHANICAL AND HANDLING

The AN221E04 comes in the industry standard 44 lead MQFP package.

Dry pack handling is recommended. The package is qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.

LQFP Package. devices manufacture from 2010 (See page 17 for older MQFP package Devices Manufactured 2002 to 2009.).



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 [.010] PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM BODY SIZE BY AS MUCH AS 0.15 [.006].
3. DRAWING CONFORMS TO JEDEC MS-028 REV. D.
4. CONTROLLING DIMENSION IN MM.

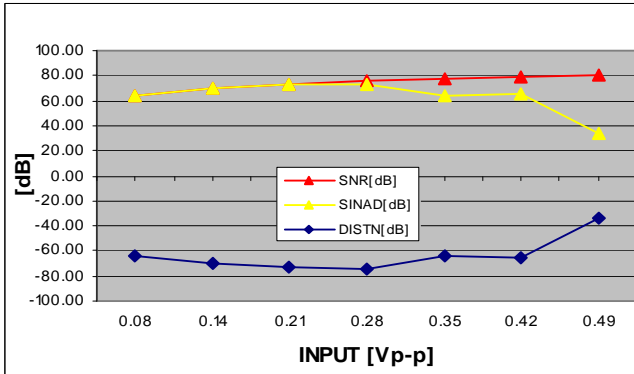
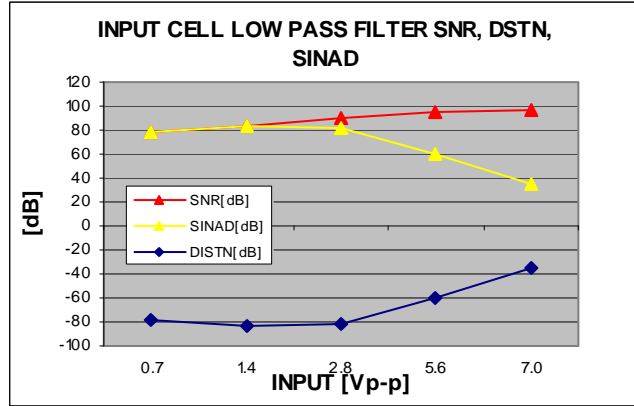
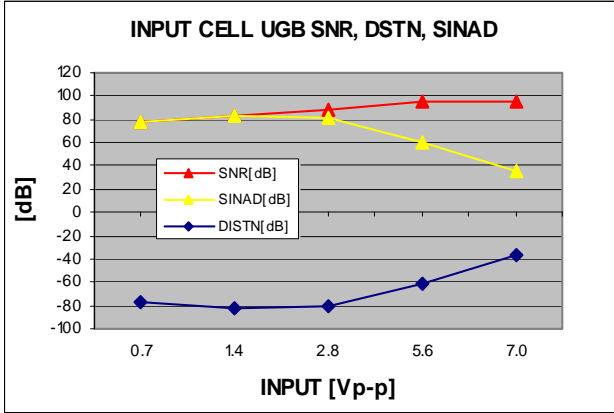


| SYMBOL | 10x10 | | |
|--------|--------------|--------------|--------------|
| | MIN | NOM | MAX |
| D | 11.8 .464 | 12 .472 | 12.2 .480 |
| D1 | 9.9 .390 | 10 .394 | 10.1 .398 |
| E | 11.8 .464 | 12 .472 | 12.2 .480 |
| E1 | 9.9 .390 | 10 .394 | 10.1 .398 |
| b | 0.3 .012 | 0.37 .015 | 0.45 .018 |
| b1 | 0.3 .012 | 0.35 .014 | 0.4 .016 |
| c | 0.09 .004 | | 0.2 .008 |
| c1 | 0.09 .004 | | 0.16 .006 |
| e | | 0.8 .031 | |
| ccc | | 0.10 .004 | |
| ddd | | 0.20 .008 | |
| N | | 44 | |
| N/2 | | 22 | |
| N/4 | | 11 | |

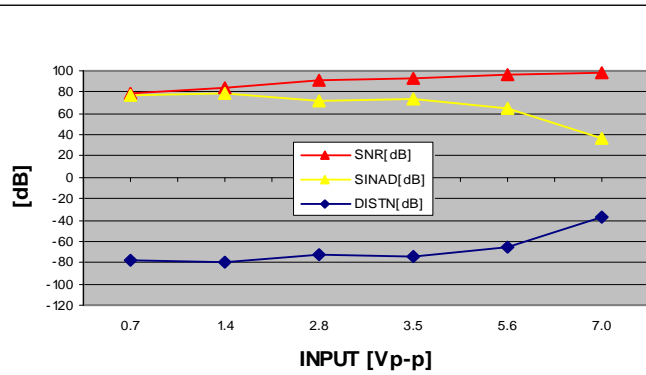
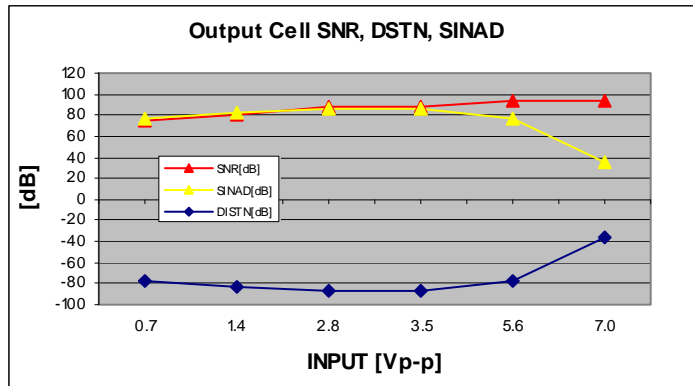
AN220E04 Datasheet – Dynamically Reconfigurable FPAA

Distortion, SINAD and SNR Measurements

The following plots give an indication of the Distortion, SINAD and SNR for some representative CAMs.



INPUT CELL AMPLIFIER SNR, DSTN, SINAD
 Measured with Inputcell Gain G = 16
 Same results for Input Amplifier and Chopper Amplifier stage, If the signal from the chopper Amplifier is correctly filtered before measurement.



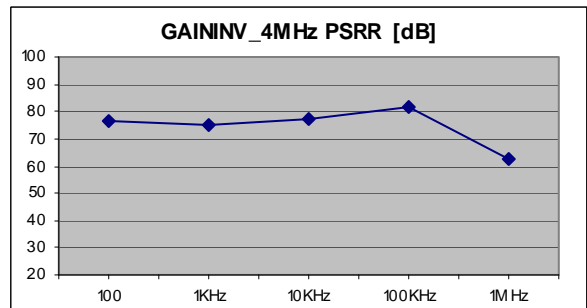
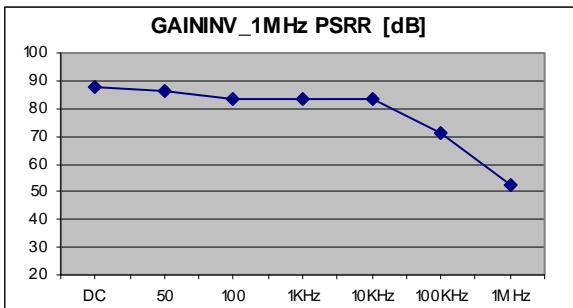
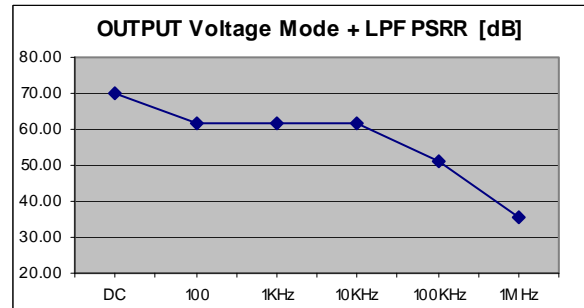
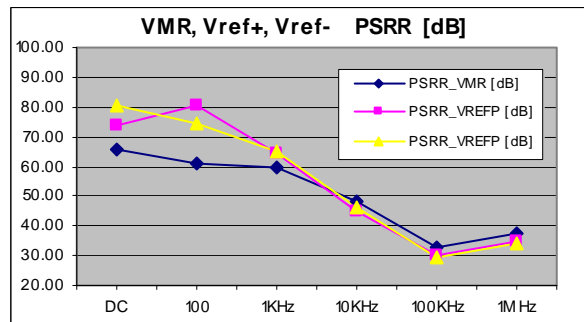
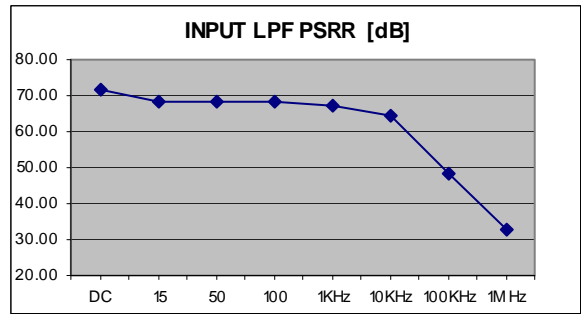
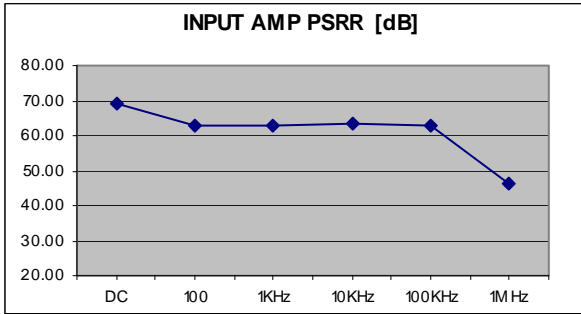
GAININV CAM SNR, DSTN, SINAD
 This graph shows the typical performance of an FPAA CAB when configured with a CAM in this example GainInv CAM
 Input signal=1400 mVp-p differential,
 CAM clock = 1MHz CAM parameter settings Gain = 1

AN220E04 Datasheet – Dynamically Reconfigurable FPAA

Power Supply Rejection Ratio (PSRR) Measurements

The following plots give an indication of the PSRR for some representative CAMs.

AVDD to Power Supply (PS): 5v +/- 0.25v sinusoidal waveform (100 kHz to 1 MHz)



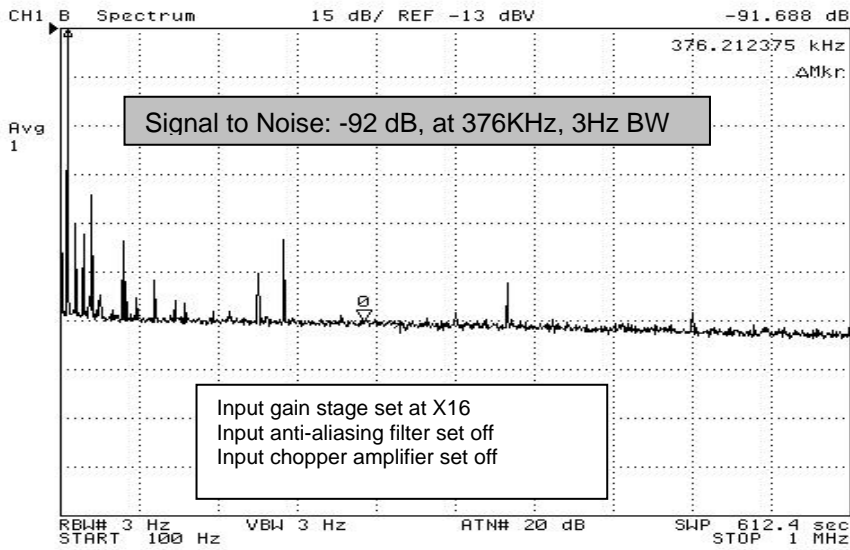
AN220E04 Datasheet – Dynamically Reconfigurable FPAA

The following is provided for information only, as and when additional characterization data is collected 'noise measurements' will be added formally to the datasheet.

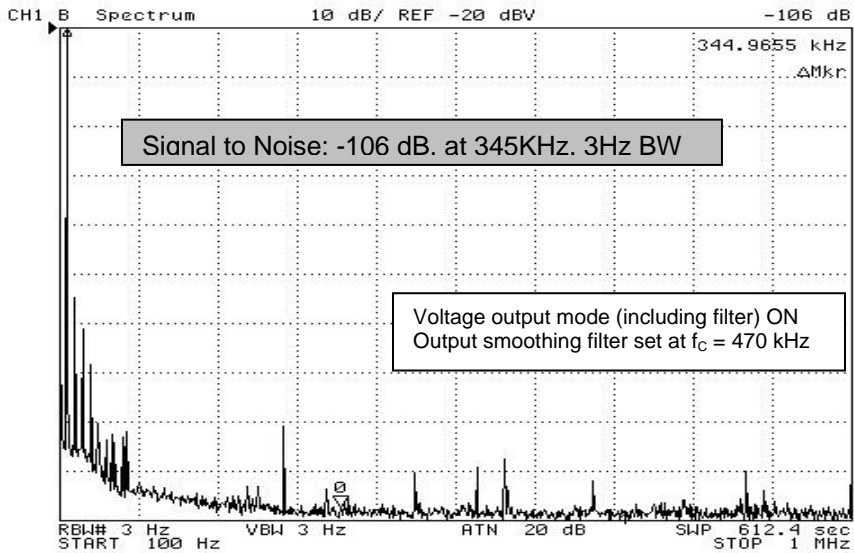
Noise And Distortion Observations

The following plots give an indication of the noise characteristics of Anadigm®'s AN220E04 FPAA device. These were done using a simple set-up and in many cases reflect the noise limit of the setup. Actual device noise margins are expected to be better.

Signal and Noise for the Input Cell (input signal - 50mVp-p differential to the FPAA at 10 kHz)



Signal and Noise for the Output Cell (with a differential input 4V p-p, 660Hz)

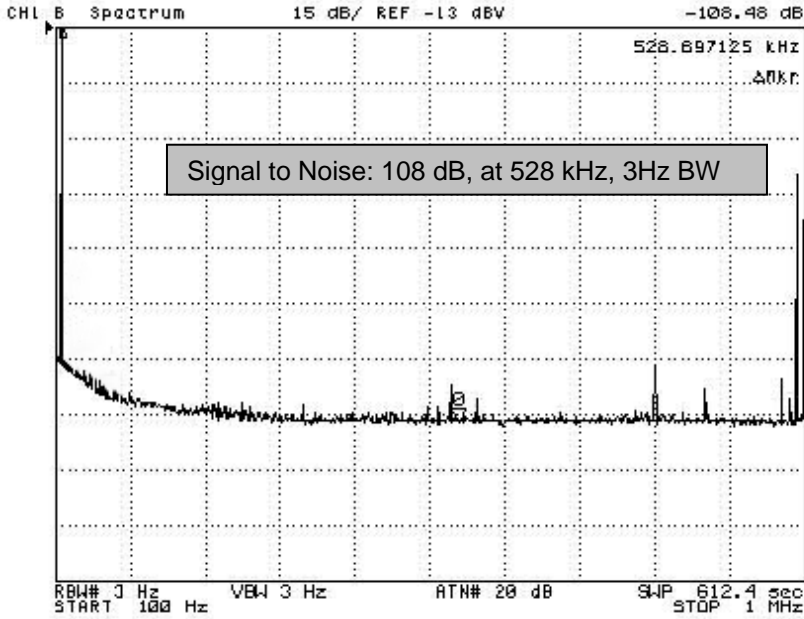


AN220E04 Datasheet – Dynamically Reconfigurable FPAA

Measured THD for input and output cells (with a differential input 4V p-p, 660Hz)

| Settings | Distortion in dB |
|--|------------------|
| Input cell with anti-aliasing filter set at $f_c = 470$ kHz | 81.6 |
| Output cell with differential to single ended converter and output smoothing filter set at $f_c = 470$ kHz | 82 |

Signal and Noise for a representative CAM – Gaininv CAM (input signal of 700mV p-p differential at 10 kHz)



THD for a representative CAM – Gaininv CAM (with a differential input 4V p-p, 660Hz)

| CAM Clock Frequency | Distortion (dB) |
|---------------------|-----------------|
| 250 KHz | 80.00 |
| 1 MHz | 72.83 |
| 2 MHz | 69.22 |
| 4 MHz | 73.48 |

