Preliminary Product Brief

FilterMaster1™
Universal Programmable Filter
6th Order, DC up to 600kHz with Gain

Anadigm's FilterMaster™ is the first of a family of chipsets from Anadigm using its dynamically programmable Analog Signal Processor (dpASP) plus State Machine to realize a dynamically programmable universal analog filter. This first application solution realizes 6th order filters, Low pass, band pass, high pass or band stop circuits can be configured with filters approximating to Butterworth, Bessel, chebyshev or inverse chebyshev. Further there are two pass/stop band widths for the band pass and band stop filters and the ability to configure the circuit to bypass mode which provides a flat unfiltered response.
It consists of a choice of 2 fixed input stages which can be configured using external resistors and capacitors to provide any or all of the following: gain or attenuation, level shifting, single-ended to differential conversion, 1st order lowpass or highpass filtering. In addition within the core of the dpASP device there is 6th order filter which can be programmed via a simple 16 bit control word, either statically by hardwiring or setting DIP switches on 16 inputs, or dynamically from a controller using a 16 bit data bus.
Both gain and stop band frequency can be dynamically programmed on the fly WITHOUT interruption to the signal. In addition, the user can select between one of two inputs, or both inputs summed, or both inputs disconnected. The outputs are fully differential for greater immunity to noise and supply ripple.
Power in operation is typically 200mW and there is a low current standby mode.

FilterMaster1™ Features

- 128 Programmable stop band frequency for each input clock frequency (input clock is user defined). These frequencies settings are arranged in octaves with 8 settings/octave or 9% spacing or step size.
- Programmable stop band frequency from DC upto 500kHz low pass, 100kHz high pass, 600kHz band pass, 120kHz band stop
- Programmable gain – 8 settings in 3dB steps
- Frequency and gain programmable without signal interruption.
- 4 Filter types – Butterworth, Chebyshev, Inverse Chebyshev (0.5dB passband ripple) and Bessel.
- Extremely simple to use 16 pin programming interface for static or dynamic programming.
- 2 input stages configurable using external resistors and capacitors for optimum signal interfacing and additional filter.
- Differential or single-ended signal input
- Fully differential analog signal outputs for better immunity to noise and supply ripple

Filter Topology and approximation Availability chart	Lowpass	Highpass	Bandpass	Bandstop
Butterworth	✓	✓	×	×
Bessel	✓	✓	✓	✓
Chebyshev	✓	✓	×	×
Inverse Chebyshev	×	×	✓	✓

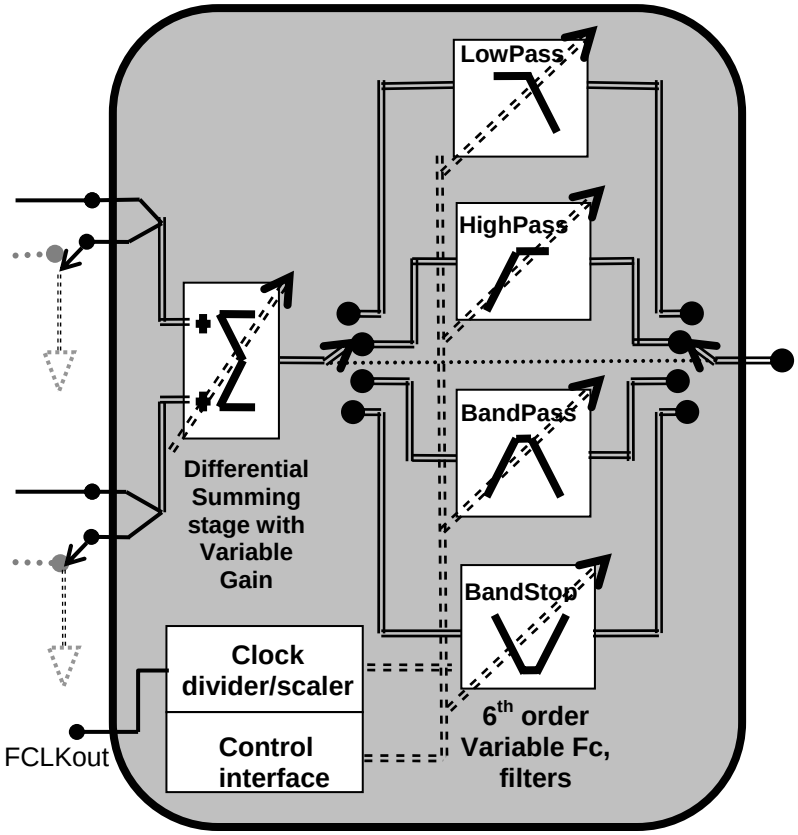
Filter variables Availability chart	Lowpass	Highpass	Bandpass	Bandstop
8 values of Fc/octave	✓	✓	✓	✓
Selectable 1 or 2 inputs with summing stage	✓	✓	✓	✓
Gain selection Mute to 18db in 3dB steps	✓	✓	✓	✓
Maximum Fc (kHz)	500	100	600	120
Wide and narrow filter	-	-	✓	✓

FilterMaster™ Benefits

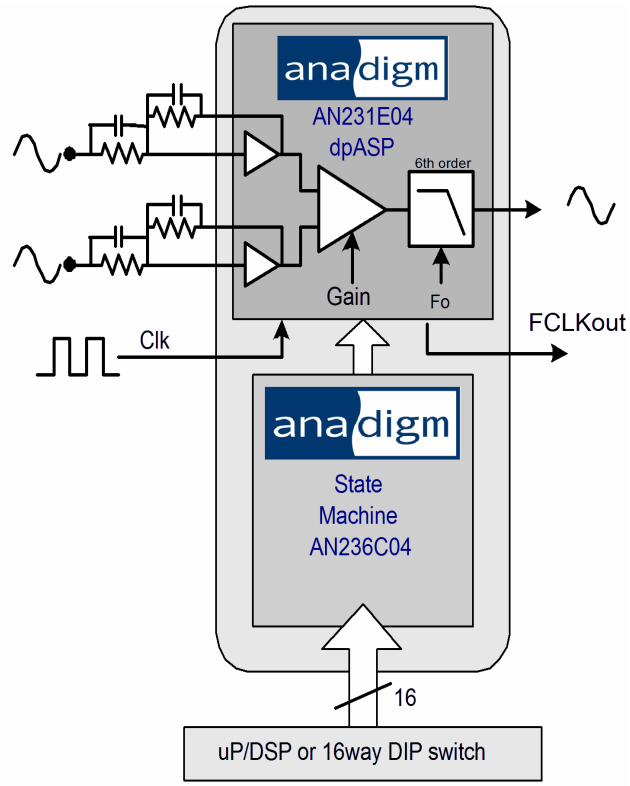
Gain and Frequency dynamically programmable without signal interruption	Low operational power 190mW, low standby current 20mW
Extremely simple to use programming interface	Easy interfacing to analog signals
Choice of filter topology and approximations	Reduced number of system components

dpASP Sub Module - Analog signal path

(Functionally equivalent drawing)



FilterMaster1 Solution uses two chips



To calculate the corner or center frequency of any filter use the following equation

CORNER FREQUENCY = (F(aclk) / "Divisor_B") * "Divisor_A" * "Divisor_C"

F(aclk) is the external clock frequency applied to the AN231E04 device ACLK pin, pin number 34.
Divisor A, B and C, see table below.

FilterMaster1 (lower 8 bits of the 16 Bit Configuration Word)

Divisor_B *Internal Clock divider settings, (divider to scale Fc in octave steps)*				**Divisor_A** *Filter Fc settings (9% steps across octave)*			**Divisor_C** *Filter topology max Fc factor*	
B4	**B3**	**B2**	**B1**	**A3**	**A2**	**A1**		
C6	C5	C4	C3	C2	C1	C0		
Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19		
B4,B3,B2,B1		**DivisorB**		**A3,A2,A1**		**DivisorA**		
0000		1		000		1.0	low pass	0.05
0001		2		001		0.917	High Pass	0.01
0010		4		010		0.841	Bandpass	0.05
0011		8		011		0.771	Bandstop	0.03
0100		16		100		0.707		
0101		32		101		0.648		
0110		64		110		0.595		
0111		128		111		0.545		
1000		256						
1001		512						
1010		1024						
1011		2048						
1100		4096						
1101		8192						
1110		16384						
1111		32768						

ANADIGM FilterMaster1 Control Interface (16 Bit Configuration Word)

Gain Settings			Analog Input Pin settings		Filter Topology		Filter approximation		DivisorB *Internal Clock divider settings, (divider to scale Fc in octave steps)*				DivisorA *Filter Fc settings (9% steps across octave)*		
MSB															LSB
G3	G2	G1	I2	I1	T4	T3	T2	T1	B4	B3	B2	B1	A3	A2	A1
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19

G3,G2,G1	Gain (dBs)
000	-infinity (Mute)
001	0.0
010	3.0
011	6.0
100	9.0
101	12.0
110	15.0
111	18.0

I2,I1	Active input(s)
00	None
01	Input A
10	Input B
11	A & B *Note1*

T4,T3	Filter topology
00	Lowpass
01	Highpass
10	Bandpass
11	Bandstop

The Filter Approximation applied depends upon the Filter topology selected.

See Table insert to the lower left

B4,B3,B2,B1	DivisorB
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

A3,A2,A1	DivisorA
000	1.0
001	0.917
010	0.841
011	0.771
100	0.707
101	0.648
110	0.595
111	0.545

Filter Approximation Applied		T4,T3	T2,T1	Comme	Width	Limits (FCLK = ACLK / DivisorB)
Lowpass	Butterworth	00	00		n/a	Max Fc = 400kHz @ FCLK(max) = 8MHz
Lowpass	Chebyshev	00	01		n/a	Max Fc = 500kHz @ FCLK(max) = 10MHz
Lowpass	Bessel	00	10		n/a	Max Fc = 250kHz @ FCLK(max) = 5MHz
Lowpass	Bypass	00	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Highpass	Butterworth	10	00		n/a	Max Fc = 60kHz @ FCLK(max) = 6MHz
Highpass	Chebyshev	10	01		n/a	Max Fc = 100kHz @ FCLK(max) = 10MHz
Highpass	Bessel	10	10		n/a	Max Fc = 50kHz @ FCLK(max) = 5MHz
Highpass	Bypass	10	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Bandpass	Inverse Chebyshev	01	00	narrow	10%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	01	01	narrow	10%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandpass	Inverse Chebyshev	01	10	wider	40%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	01	11	wider	40%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandstop	Inverse Chebyshev	11	00	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	01	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Inverse Chebyshev	11	10	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	11	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz

Notes

1) If inputs A and B are selected then the two active input signals will be summed.

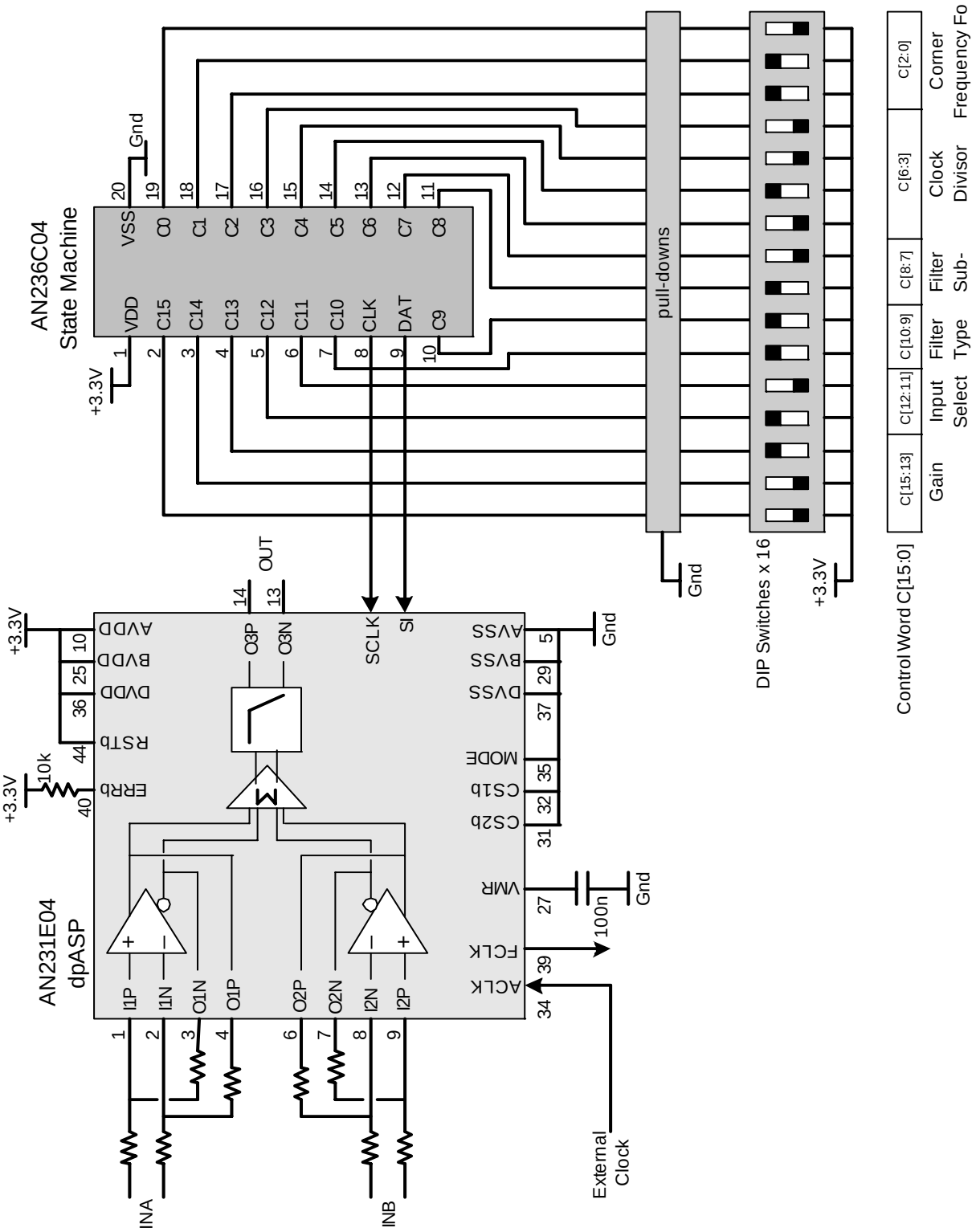
2) Setting of five 0's for the control bits C[15:11] (zero gain and no inputs selected) causes the FPAA to be reset and FilterMaster to go into standby (approx 6mA from 3.3volts)

3) Max Fc, or maximum Filter Corner or Center Frequency limits have been determined for better than 1% accurate filter parameters, exceeding these limits will result in loss of filter accuracy.

*4) Bypass filter approximation provides a flat response from d.c. to FCLK * 0.1. (FCLK = ACLK / Divisor_B). Divisor_A inputs have no effect in this mode, gain and input select still apply.*

5) Divisor_A step size is mathematically equal to (8thsqrt(2) or ((2)^^(1/8).

6) FCLK (= ACLK / DivisorB) is provided on an output pin from the AN231E04, the primary purpose of this signal is to enable synchronization of any subsequent ADC,



Product codes

Evaluation Kit	AN236K04-EVAL2
Sample Chipset	AN236K04-SETSP (contains 1 x AN231E04-QFNSP and 1 x AN236C04-SSOSP)
Volume Chipset	AN236K04-SETTY (contains 1 x AN231E04-QFNTY and 1 x AN236C04-SSOTU)

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