AnadigmFilter1 Evaluation Board Quick Start User Guide

PLEASE read all of this minimal document before starting. It may save you a lot of time.

Figure 1 below shows a photo of the AnadigmFilter1 Evaluation Board.

Figure 1.

Quick start instructions:

1. Power up the board by connecting it to a +3.3V power supply.
2. Connect a ground referenced differential signal to INA+ and INA-. If the signal is single-ended, connect it to INA+ and connect INA- to ground.
3. Set configuration bits C13 and C11 high. This will enable input port A and set the gain to 0dB (x1).
4. Monitor the differential output on OUT+ and OUT-. The output signal will be filtered by a lowpass Butterworth filter with corner frequency 400kHz. See below for details of how to calculate corner frequency for different configuration settings and different master clock frequencies.

To calculate the corner or center frequency of any filter use the following equation

CORNER FREQUENCY = (F(aclk) / "Divisor_B") * "Divisor_A" * "Divisor_C"

F(aclk) is the external clock frequency applied to the AN231E04 device ACLK pin.
Divisor A, B and C, see table below.

AnadigmFilter1 (lower 8 bits of the 16 Bit Configuration Word)

Divisor_B *Internal Clock divider settings, (divider to scale Fc in octave steps)*				**Divisor_A** *Filter Fc settings (9% steps across octave)*			**Divisor_C** *Filter topology max Fc factor*	
B4	**B3**	**B2**	**B1**	**A3**	**A2**	**A1**		
C6	C5	C4	C3	C2	C1	C0		
Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19		
B4,B3,B2,B1		**DivisorB**		**A3,A2,A1**		**DivisorA**		
0000		1		000		1.0	low pass	0.05
0001		2		001		0.917	High Pass	0.01
0010		4		010		0.841	Bandpass	0.05
0011		8		011		0.771	Bandstop	0.03
0100		16		100		0.707		
0101		32		101		0.648		
0110		64		110		0.595		
0111		128		111		0.545		
1000		256						
1001		512						
1010		1024						
1011		2048						
1100		4096						
1101		8192						
1110		16384						
1111		32768						

5. The board comes with an 8MHz oscillator module. This can be replaced by another or disabled and an external clock applied to the CLK IN pin. The oscillator module can be disabled by applying a jumper or short to J3. Note: stopping the external clock makes the filter go into deep sleep mode (~20uW) regardless of control word setting.
6. The filter clock is output on pin CLK OUT. The filter clock is the master clock divided by Divisor_B.
7. Set C11 low and C12 high. The input signal can now be applied to input port B. If both C11 and C12 are high then signals on both port A and port B will be summed.
8. Configuration bits C13 – 15 allow adjustment of the gain from 0dB to 18dB in 3dB steps.
9. If jumpers are applied to J1 and J2 then the output capacitors will be shorted. This means that the differential output signal will have a common mode voltage level of +1.5V.
10. See the table called "AnadigmFilter1 Control Interface" later in this document for details on how to set the different filter types and the limiting frequency for each type.
11. The input stages (see fig 3 and also schematic) consist of through hole capacitors (C10-17) and resistors (R19-26) combined with the input opamp of the dpASP. This input stage can be configured by the user to provide fixed filtering, gain and voltage step-up. The dpASP uses +1.5V centered signals but the input stages allow the user to drive the board with ground referenced signals. The through-hole resistors provided are 10k ohm and give a gain of x1. Note that the dpASP cannot be driven by a signal whose differential amplitude is greater than +/-3V (because signals on its pins IxP & IxN must be between 0 and +3V) so if the signal to the board is greater than +/-3V then the input stage should be configured to give a gain of < x1 (e.g. i/p +/-6V, make gain x0.5). The capacitors are not populated but can be added by the user to provide the desired (fixed) filtering on the input stage e.g. adding feedback caps to C12,13 or C16,17 will make a lowpass input filter (formula for Rs & Cs is standard).

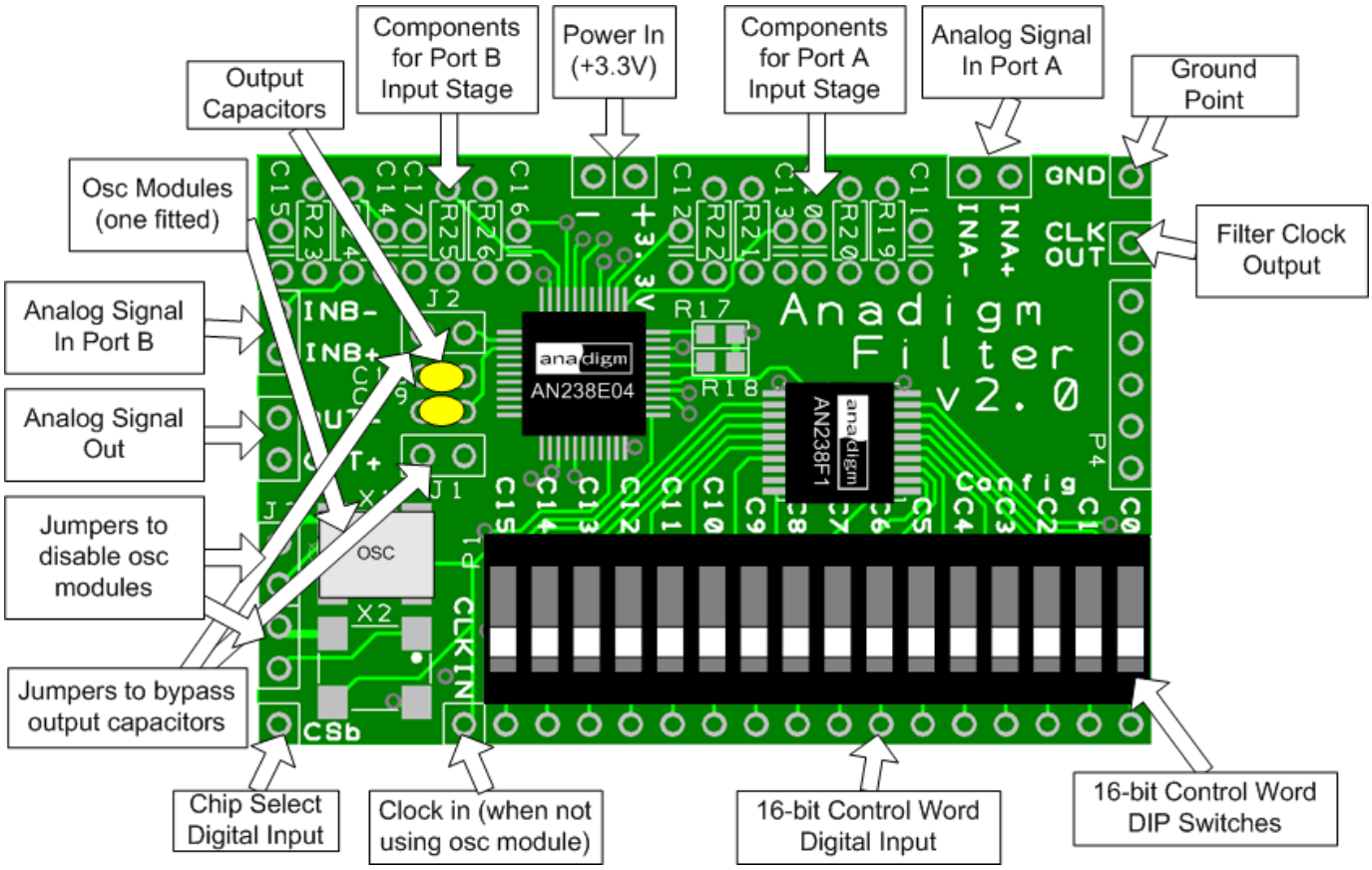


Figure 2, Pictorial Pin description

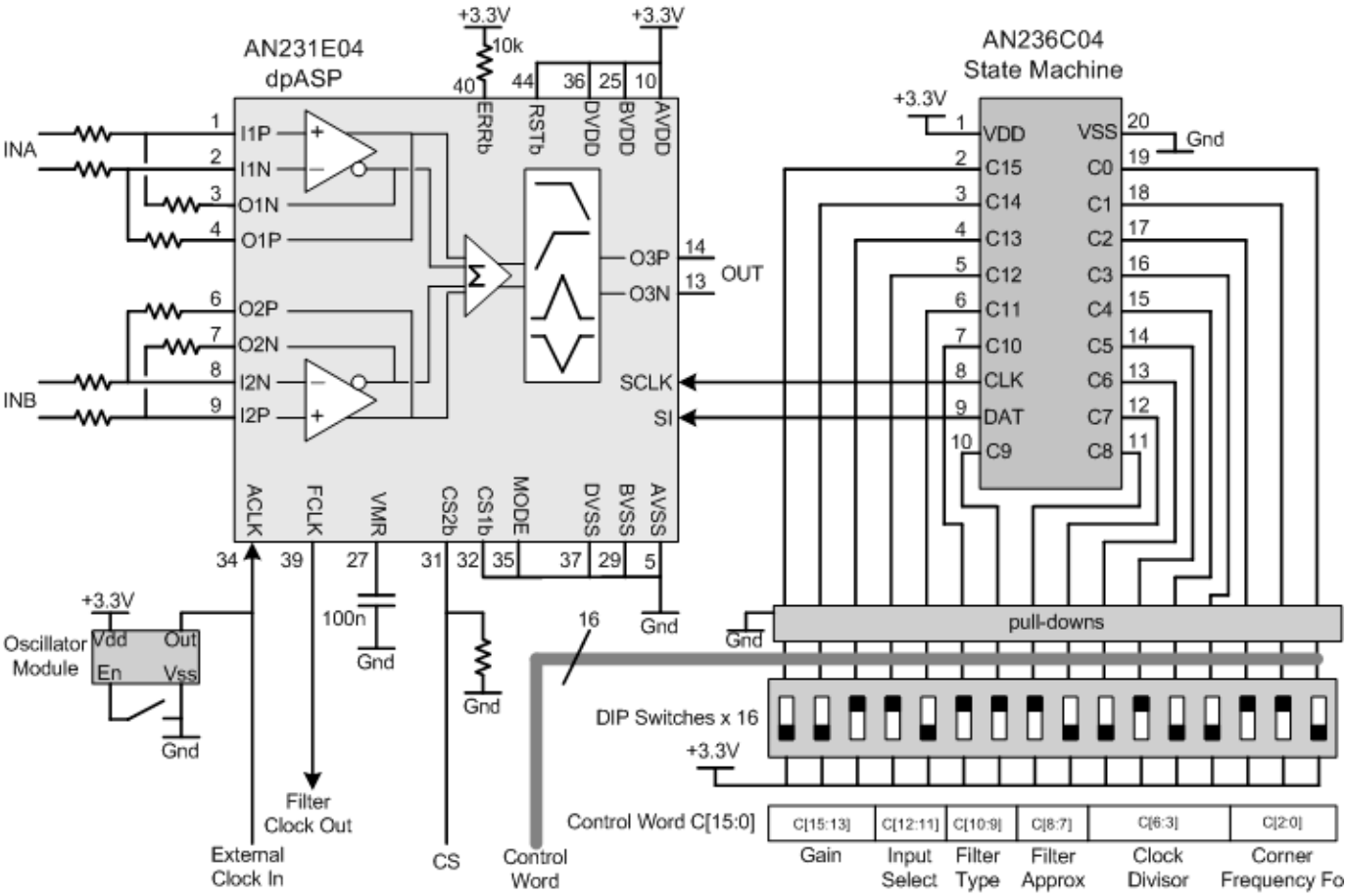
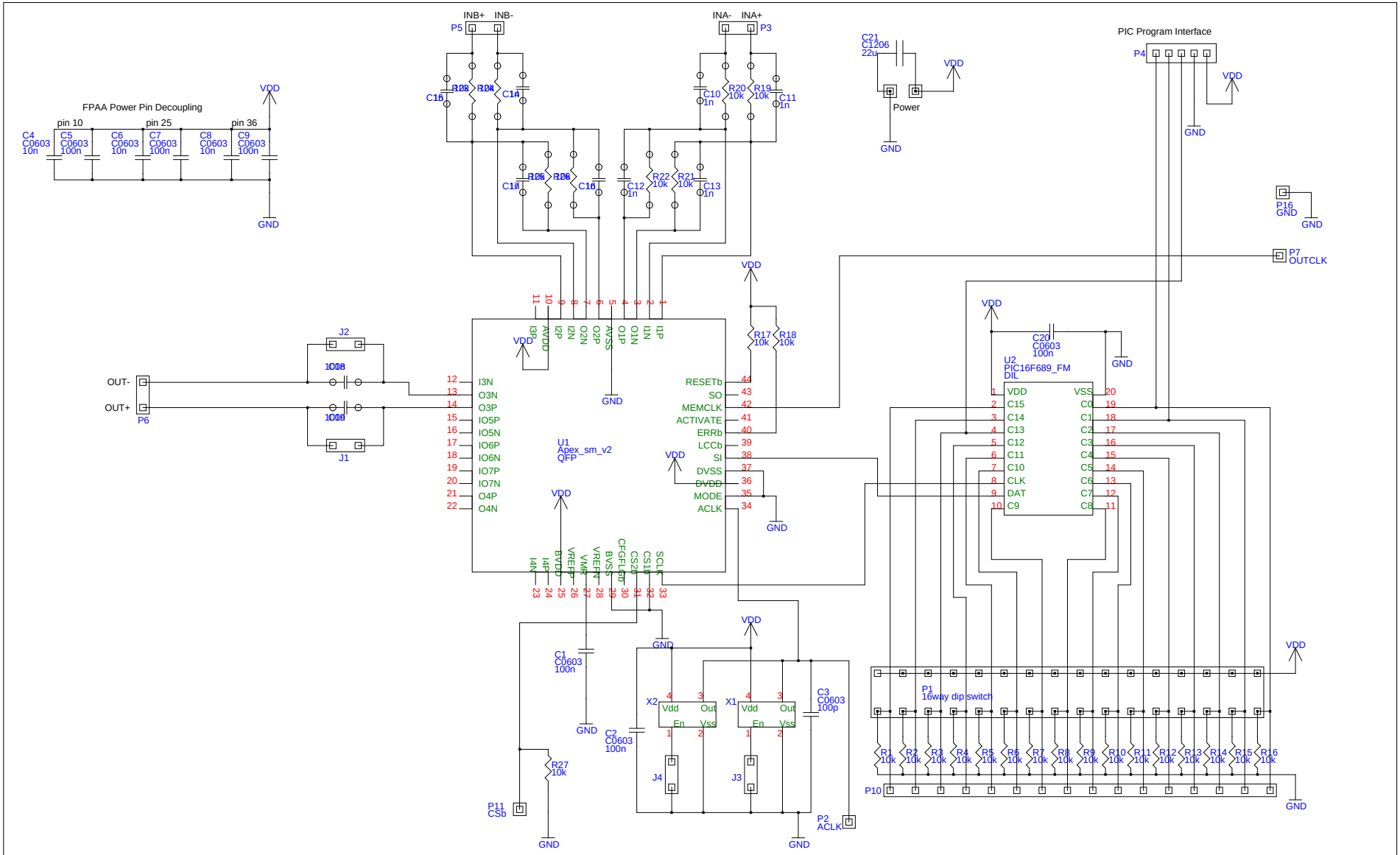


Figure 3, Block Diagram



E	D	C	B	A	Drawn	Check	Projection Do Not Scale	Anadigm FilterMaster Board v2.0
Drn	Drn	Drn	Drn	Project			Client	
Chk	Chk	Chk	Chk	Title			Filename	Drawing No. Dave Lovell Oct 22nd 2009 / Sheet of

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ANADIGM AnadigmFilter1 Control Interface (16 Bit Configuration Word)

Gain Settings			Analog Input Pin settings		Filter Topology		Filter approximation		DivisorB *Internal Clock divider settings, (divider to scale Fc in octave steps)*				DivisorA *Filter Fc settings (9% steps across octave)*		
MSB															LSB
G3	G2	G1	I2	I1	T4	T3	T2	T1	B4	B3	B2	B1	A3	A2	A1
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 10	Pin 11	Pin 12	Pin 13	Pin 14	Pin 15	Pin 16	Pin 17	Pin 18	Pin 19

G3,G2,G1	Gain (dBs)
000	-infinity (Mute)
001	0.0
010	3.0
011	6.0
100	9.0
101	12.0
110	15.0
111	18.0

I2,I1	Active input(s)
00	None
01	Input A
10	Input B
11	A & B *Note1*

T4,T3	Filter topology
00	Lowpass
01	Highpass
10	Bandpass
11	Bandstop

The Filter Approximation applied depends upon the Filter topology selected.

See Table insert to the lower left

B4,B3,B2,B1	DivisorB
0000	1
0001	2
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

A3,A2,A1	DivisorA
000	1.0
001	0.917
010	0.841
011	0.771
100	0.707
101	0.648
110	0.595
111	0.545

Filter Approximation Applied		T4,T3	T2,T1	Commen	Width	Limits (FCLK = ACLK / DivisorB)
Lowpass	Butterworth	00	00		n/a	Max Fc = 400kHz @ FCLK(max) = 8MHz
Lowpass	Chebyshev	00	01		n/a	Max Fc = 500kHz @ FCLK(max) = 10MHz
Lowpass	Bessel	00	10		n/a	Max Fc = 250kHz @ FCLK(max) = 5MHz
Lowpass	Bypass	00	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Highpass	Butterworth	01	00		n/a	Max Fc = 60kHz @ FCLK(max) = 6MHz
Highpass	Chebyshev	01	01		n/a	Max Fc = 100kHz @ FCLK(max) = 10MHz
Highpass	Bessel	01	10		n/a	Max Fc = 50kHz @ FCLK(max) = 5MHz
Highpass	Bypass	01	11		n/a	Max Fc = 1000kHz @ FCLK(max) = 10MHz
Bandpass	Inverse Chebyshev	10	00	narrow	10%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	10	01	narrow	10%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandpass	Inverse Chebyshev	10	10	wider	40%	Max Fc = 500kHz @ FCLK(max) = 10MHz
Bandpass	Bessel	10	11	wider	40%	Max Fc = 600kHz @ FCLK(max) = 12MHz
Bandstop	Inverse Chebyshev	11	00	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	01	narrow	20%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Inverse Chebyshev	11	10	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz
Bandstop	Bessel	11	11	wider	80%	Max Fc = 120kHz @ FCLK(max) = 4MHz

Notes

1) If inputs A and B are selected then the two active input signals will be summed.

2) Setting of five 0's for the control bits C[15:11] (zero gain and no inputs selected) makes AnadigmFilter go into standby (approx 20mW). Stopping the external clock makes dpASP go into deep sleep (< 20uW).

3) Max Fc, or maximum Filter Corner or Center Frequency limits have been determined for better than 1% accurate filter parameters, exceeding these limits will result in loss of filter accuracy.

*4) Bypass filter approximation provides a flat response from d.c. to FCLK * 0.1. (FCLK = ACLK / Divisor_B). Divisor_A inputs have no effect in this mode, gain and input select still apply.*

5) Divisor_A step size is mathematically equal to (8thsqrt(2) or ((2)^^(1/8).

6) FCLK (= ACLK / DivisorB) is provided on an output pin from the AN231E04, the primary purpose of this signal is to enable synchronization of any subsequent ADC