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***The FPAA Company***  
*Field Programmable Analog Arrays*  
*real time Analog programmability*

2016 Technical Training, Class IV



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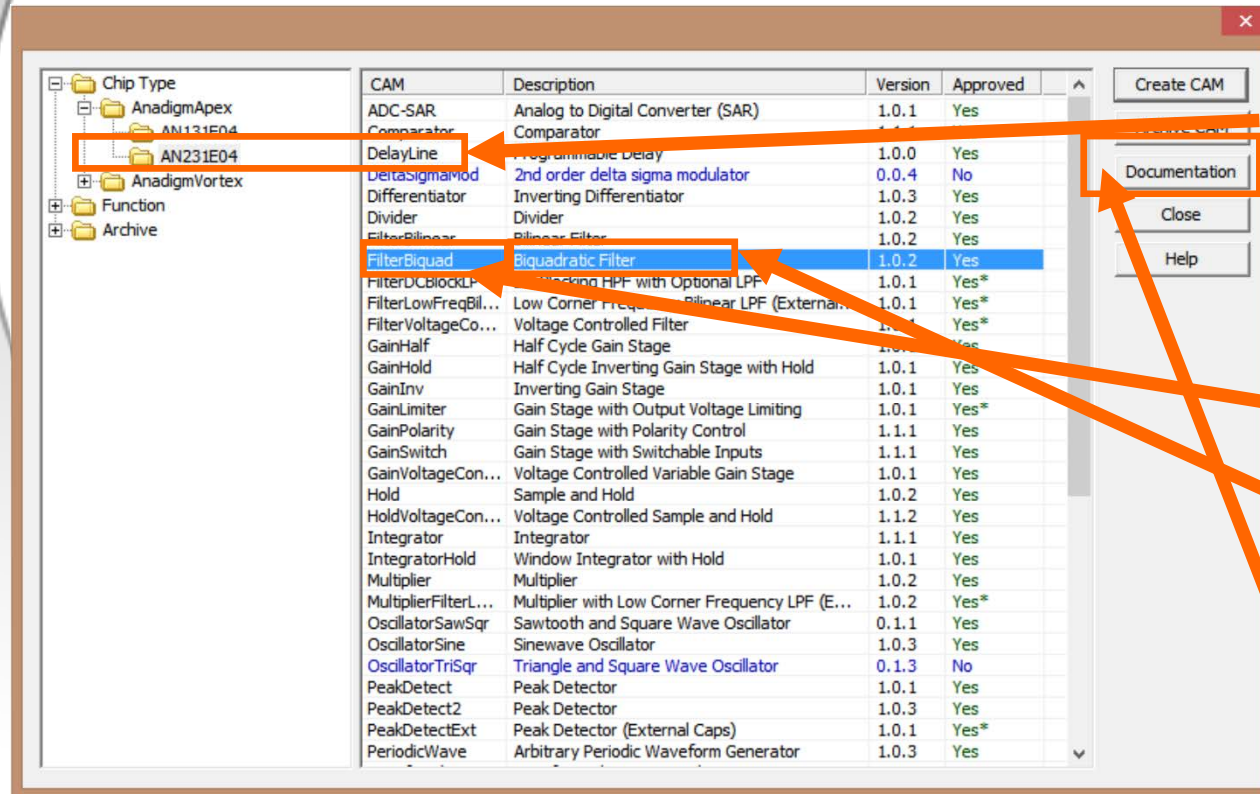
## What is a Configurable Analog Module (CAM)?

- **Circuit building blocks abstracted to a functional level that can be manipulated in AnadigmDesigner<sup>®</sup> 2**
- **A complex circuit can be implemented in a “chip” simply by selecting, configuring, placing and wiring CAMs**
- **Improved speed and ease of circuit design**

# AnadigmDesigner® 2 CAMs

- **Very dynamic – powerful yet easy to use**
  - Multiple circuit topologies – CAM knows how to make what you ask for
  - Dynamic user interface – options and limits can change
    - Allows user to push the limits of the CAM
    - Constrains the user to legal configurations
- **Expanded CAM documentation explains the features**

# Selecting a CAM



- **Library**
  - AnadigmApex
    - AN231E04
- **Name**
  - FilterBiquad
- **Description**
  - Biquadratic Filter
- **Documentation**

**In AnadigmDesigner<sup>®</sup>2, CAMs may contain multiple circuit configurations. Select the basic function. The details will be set during CAM configuration.**

# Configuring the CAM - Information

Set CAM Parameters

Instance Name: **FilterBiquad2** AnadigmApex FilterBiquad 1.0.2 (Biquadratic Filter)

Clocks: ClockA: Clock0 (4000 kHz)

\*This is an inverting filter.\* See the transfer function in the CAM Documentation.

**Options**

Filter Type:  Low Pass  High Pass

Filter Topology:  Automatic  Type 1

Input Sampling Phase:  Phase 1  Phase 2

Polarity:  Inverting  Non-inverting

Opamp Chopping:  Enabled

**Parameters**

Corner Frequency [kHz]: 40 (40.0 realized) [8.000 to 80.000]

Gain: 1 (1.00 realized) [0.100 to 10.000]

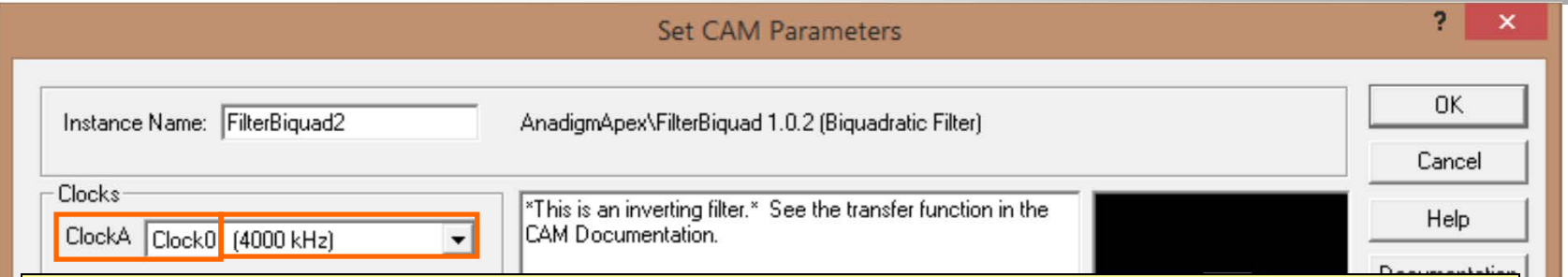
Quality Factor: 0.707 (0.707 realized) [0.0600 to 70.0]

CAM Source: Anadigm Approved: **Yes**

Buttons: OK, Cancel, Help, Documentation, Code...

- **CAM Version Number**
  - 1.0.0
- **CAM Description**
  - Biquadratic Filter
- **Library**
  - ANx20 Standard
- **Instance Name**
  - FilterBiquad
  - Default may be changed
- **Approval Level**

# Configuring the CAM - Clocks



Set CAM Parameters

Instance Name: FilterBiquad2    AnadigmApex\FilterBiquad 1.0.2 (Biquadratic Filter)

Clocks

ClockA Clock0 (4000 kHz)

\*This is an inverting filter.\* See the transfer function in the CAM Documentation.

OK  
Cancel  
Help  
Documentation

- Set the clock(s)
  - Spinners associate CAM clocks (CLOCKA) with chip clocks (Clock 0) and show the frequency of that chip clock
  - Chip clock frequencies are set in the “Chip Settings” dialog box
- All CAMs in a signal path should use the same chip clock for the analog clock (CAM CLOCKA)
- Some CAM parameters are clock dependent (filter corner frequency)
  - These CAMs should be reconfigured if the clock frequencies are changed
- CAMs with multiple clocks contain instructions about their relation

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CAM Source: Anadigm, Approved: FCS

# Configuring the CAM - Options

Instance Name: FilterBiquad2    AnadigmApex\FilterBiquad 1.0.2 (Biquadratic Filter)

Clocks  
ClockA: Clock0 (4000 kHz)

\*This is an inverting filter.\* See the transfer function in the CAM Documentation.

**Options**

**Filter Type:**  Low Pass    High Pass    Band Pass    Band Stop    Pole and Zero

Filter Topology:  Automatic    Type I    Type II

Input Sampling Phase:  Phase 1    Phase 2

Polarity:  Inverting    Non-inverting

Opamp Chopping:  Enabled

Buttons: OK, Cancel, Help, Documentation, C Code...

- CAM Options
  - Option settings control circuit configuration. This is reflected in the symbol. Options and parameters may also change
  - Options may be gray due to incompatible combinations or unavailable resources

# Configuring the CAM - Parameters

Instance Name: FilterBiquad2    AnadigmApex\FilterBiquad2

Clocks  
ClockA: Clock0 (4000 kHz)

\*This is an inverting filter. See the CAM Documentation.

**Options**

Filter Type:  Low Pass     High Pass

Filter Topology:  Automatic     Type I

Input Sampling Phase:  Phase 1     Phase 2

Polarity:  Inverting     Non-inverting

Opamp Chopping:  Enabled

**Parameters**

Corner Frequency [kHz]:	40	(40.0 realized)	[8.00 To 400]
Gain:	1	(1.00 realized)	[0.100 To 100]
Quality Factor:	0.707	(0.707 realized)	[0.0600 To 70.0]

CAM Source: Anadigm, Approved: Yes

- Parameter Names
  - May include units
- Desired Value
  - Entered by the user
- Parameter Limits
  - Values will be restricted
- Realized Value
  - What was possible for this combination of desired values



# Parameters - Quantization and Error

Parameter:	Value:	Limits:	Realized
Gain 1 (UpperInput)	1	0.0100 To 6.55	1.00
Gain 2 (LowerInput)	0.0257	0.0100 To 100	0.0258

- Realized values show the implementation of the parameter based on ratios of programmable capacitor banks which are **quantized**

$$\frac{6 \text{ unit caps}}{233 \text{ unit caps}} = 0.02575$$

- Actual measured values can have **error** in addition to the quantization of the realized value

$$Gain_{Realized} = 0.02575$$

$$Gain_{Measured} = 0.0259 \Rightarrow 0.6 \% \text{ error}$$

# Parameters - Interrelation

Parameter:	Value:	Limits:	Realized
Gain 1 (UpperInput)	6	0.0100 To 6.55	6.00
Gain 2 (LowerInput)	0.0257	0.0235 To 100	0.0256

$$\frac{234 \text{ unit caps}}{39 \text{ unit caps}} = 6.0 \quad \frac{1 \text{ unit caps}}{39 \text{ unit caps}} = 0.02564$$

- Limits are dynamic. Changing desired values can also change the limits.
  - If Gain 1 = 6.0  
Gain 2 cannot be less than 0.0235
  - If Gain 2 = .0257  
Gain 1 cannot be greater than 6.55

- Realized values are based on the combination of capacitor ratios. Changing one desired value can change multiple realized values.

# Configuring the CAM - LUT

Set CAM Parameters

ANx20 Standard User-defined Voltage Transfer Function 1.0.0

Anadigm Approved CAM

Instance name and clock frequency

Instance Name: TransferFunction

CLOCKA (kHz): 1048.75

CLOCKB (kHz): 16780

Notes: Enter voltage transfer function profile by pressing the Lookup Table button.

Symbol:  $\Phi_1$

Dialog

Voltage Transfer Function

Limits = -4 to 4

Vin	Value	Realized
$X < -2.977$	0.000000	0.000000
$-2.977 < X < -2.953$	0.000000	0.000000
$-2.953 < X < -2.930$	0.000000	0.000000
$-2.930 < X < -2.906$	0.000000	0.000000
$-2.906 < X < -2.883$	0.000000	0.000000
$-2.883 < X < -2.859$	0.000000	0.000000
$-2.859 < X < -2.836$	0.000000	0.000000
$-2.836 < X < -2.813$	0.000000	0.000000
$-2.813 < X < -2.789$	0.000000	0.000000
$-2.789 < X < -2.766$	0.000000	0.000000
$-2.766 < X < -2.742$	3.210000	3.201681
$-2.742 < X < -2.719$	0.000000	0.000000
$-2.719 < X < -2.695$	0.000000	0.000000

- Parameter entry to set output voltages
  - Limits
  - Input voltage range that will trigger this output
  - Desired value
  - Realized value

# Configuring the CAM - Finishing

**Read any notes for help with configuration**

- Documentation
  - Online help about this CAM
- Cancel
  - Discard all changes
- OK
  - Accept all changes

# Online CAM Documentation

**Half Cycle Gain Stage**

**Hardware Compatibility**  
This CAM is compatible with the following chip types:  
AD5000A, AD5000B

**Related CAMs**  
The Galileo-CAM creates a half cycle meeting gain stage. This gain stage has continuous input and continuous output that is always valid.  
The Galileo-CAM creates a half cycle meeting gain stage with output hold. It has a sampled input and an output that is valid during both phases. The output has an input output after compensation during a single output phase. The upper gain limit may be higher than that of a Galileo-CAM.

**CAM Options: Priority**  
This is the option for a gain stage with input phase 1. Other versions are available.  
Resampling: The half cycle output is delayed by one phase (one half of a clock period) in the non-sampling version.  
Sampling: This is the option for a gain stage with input phase 1. Other versions are available.  
Phase 1: This is the option for a non-sampling gain stage. Other versions are available.  
Phase 2: This version should be considered to sample a signal in either output phase 1 or continuously valid. This is the option for a continuously valid. Other versions are available.

**CAM Parameters:**

Gain	0.00 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V
	0.00 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V	0.01 - 0.015 V/V

**Circuit Diagram and Design Equations:**  
The transfer function for the circuit is:  
$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_2}{R_1} \frac{1 + sR_2C_2}{1 + sR_1C_1}$$
  
The circuit realizing the CAM is shown at the figure at right.  
The capacitor values are chosen based on the best values of the capacitors satisfying the following relations:  
$$C_1 = \frac{C_2}{10}$$

**Switch Phasing:**

Priority	Input Sampling	SI	SI	SI	SI
Resampling	Phase 1	SI	SI	SI	SI
Sampling	Phase 1	SI	SI	SI	SI
Phase 1	Phase 1	SI	SI	SI	SI
Phase 2	Phase 1	SI	SI	SI	SI

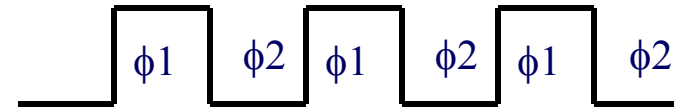
**Output Characteristics**  
The sampling version of this CAM does not have additional phase delay due to sampling in the half cycle output. The non-sampling version of this CAM exhibits one phase (one half of a clock period) of delay. Therefore the half cycle output is available one phase (one half of a clock period) after the input was sampled. The appropriate phase for input and output is shown in the circuit diagram.  
This CAM is built-in with the output phase on a relation of priority and input sampling is valid. The output will be signal ground (undefined) after each phase. Therefore the output within CAM is only valid during one phase.

- Anadigm approved CAMs contain information about CAM construction and proper usage
  - Details about each CAM option
  - Details about each CAM parameter
  - Design Equations
  - Circuit Diagrams
  - Switch Phasing
  - Output Characteristics
- Some include additional design notes with information about special features of that CAM

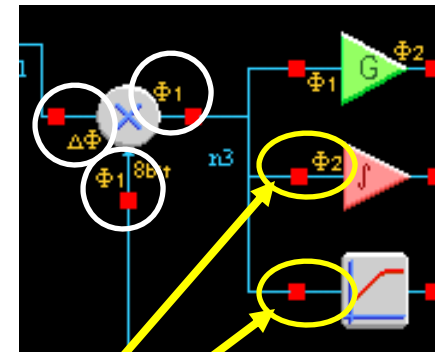
# Placing and Wiring CAMs

- **Place the CAM within the chip borders**
  - Green warning marker indicates the CAM cannot be dropped on top of something
  - Red warning marker indicates that available resources are not sufficient to implement the CAM
- **Draw wires between the CAM contacts**
  - Only legal connections will be allowed
- **Chips can be connected for simulation**

# Clock Phases



- Each clock has two non-overlapping phases
- Phase symbol on a CAM input shows an input that samples only on that phase
  - $\Delta\phi$  indicates that the sampling phase changes during operation
- Phase symbol on a CAM output shows the output should be sampled on that phase
- **Warning:** a phased output can be safely connected only to a similarly phased input
- Always see the CAM documentation for details on input/output characteristics



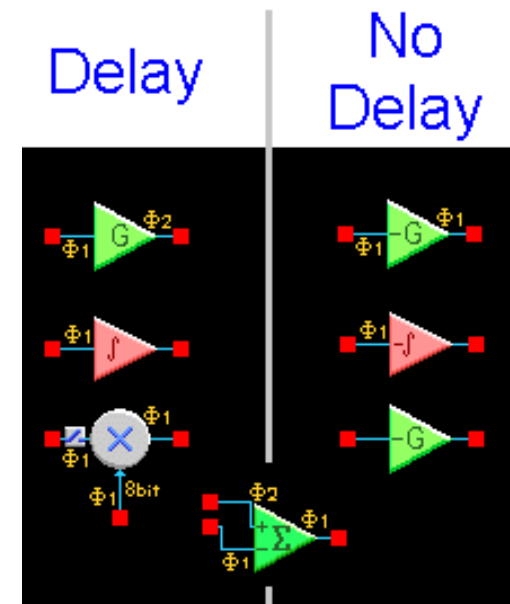
# Clock Delay

- CAMs may have signal delay due to the timing of clocked switches. This is not the same as filter phase delay.
- Clock delay can often be neglected if the clock frequency is adequately higher than the signal frequency

Example – 10 kHz signal CAM  
has half clock cycle delay

- With 50 kHz clock  
36 degree delay (possibly significant)
- With 1 MHz clock  
1.8 degree delay (probably negligible)

- Clock delay is not shown by symbol alone
- Always see the CAM documentation for details on input/output characteristics





# CAM Files

## .cam File

- **Primary CAM file**
- **ASCII based**
- **Read directly by AnadigmDesigner<sup>®2</sup>**
- **Strictly formatted, keyword driven with very little error checking**

Name, Version, User Interface  
Control, Circuit Definition,  
Parameter Calculation, Symbol,  
Simulation equations, CCODE, etc.

## .chm File

- **CAM Documentation or Help file**
- **Compiled HTML**
- **Referenced and displayed by AnadigmDesigner<sup>®2</sup>**

# CAM Gain Elements

There are four basic gain topologies that are reused in many CAMs (gain stage, rectifier, summing stage, etc)

- **xxxInv**

- Inverting
- Continuous time – the input is not sampled

- **xxxHalf**

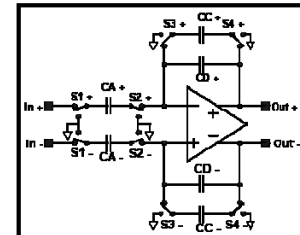
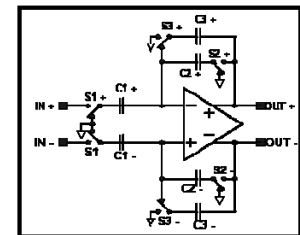
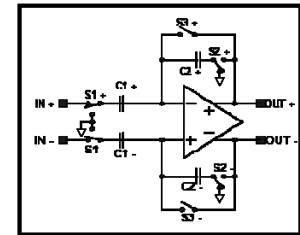
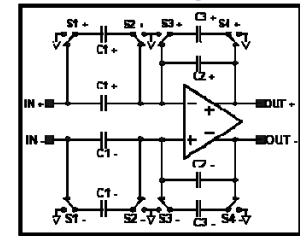
- Inverting or non-inverting
- Amplifier input offset compensation
- Half-cycle (Output is zero during one phase)
- Subject to clock frequency/gain limitations

- **xxxHold**




- Inverting
- Amplifier input offset compensation for only one phase

- **xxxFilter** – uses a single pole low pass filter

- Inverting or non-inverting

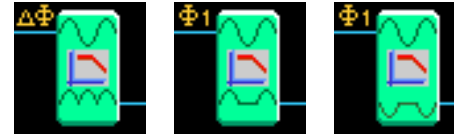


# ANx20 Standard Library – Gain Stages

- **GainHalf** 
  - Half-cycle
- **GainHold** 
  - Inverting only
- **GainInv** 
  - Continuous Time

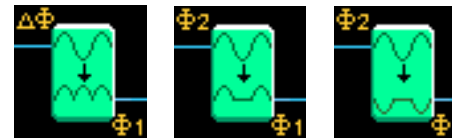
# ANx20 Standard Library – Rectifiers

- **RectifierFilter**



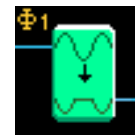
- Full Wave/Half Wave
- Inverting/non-inverting

- **RectifierHalf**



- Full Wave/Half Wave
- Inverting/non-inverting

- **RectifierHold**



- Half Wave Inverting only

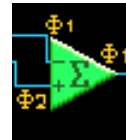
# ANx20 Standard Library – Summing

- **SumInv**



- Up to three inputs

- **SumDiff (SumHalf)**



- Up to four inputs
- Add or subtract since input branches can be inverting or non-inverting

# ANx20 Standard Library – Filters

- **FilterBilinear – One pole**



- Low Pass/High Pass/All Pass

- **FilterBiquad – Two poles**



- Low Pass/High Pass/Band Pass/Band Stop
- Automatically chooses from multiple circuit topologies



**Some other CAMs use a low pass bilinear filter as part of another function (RectifierFilter)**

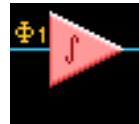
# ANx20 Standard Library – Math

- **Differentiator**

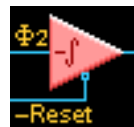


- Output voltage slews – see documentation

- **Integrator**



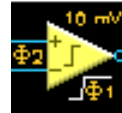
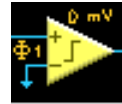
- Optional reset



# ANx20 Standard Library

- **Comparator**

- Single/Dual Input
- Variable Reference



- **Hold – Sample and hold**



- **OscillatorSine**



- Subject to internal reference voltage error

- **Voltage (+/- 3 VDC)**

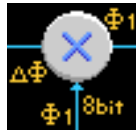


- Subject to internal reference voltage error

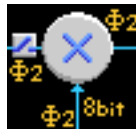


# ANx20 Standard Library – Multiplier

- **Multiplier**



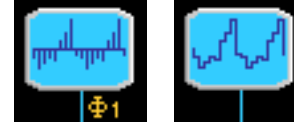
- Uses SAR (Input Y is quantized)
- Subject to internal reference voltage error
- Optional sample and hold on input X to equalize sampling time of two inputs (uses chip resources)



# ANx20 Standard Library – LUT

- **PeriodicWave**

- Half-cycle/Output Hold



- Uses LUT to generate a user-defined periodic sequence of output voltages
- Documentation has help with loading the LUT

- **TransferFunction**

- Half-cycle/Output Hold



- Uses the SAR and LUT to perform A/D conversion on the input and generate the appropriate user-defined output voltage