Application Note: AnadigmApex RMS to DC Converter

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1 Purpose

This application note describes how to use the Delta Sigma Modulator CAM (xDeltaSigmaMod v0.0.9) as part of an RMS to DC converter. This CAM can be exploited to create higher performance systems when compared to those which use the Multiplier and Divider CAMs employing the 8-bit SAR.

The reader is introduced to the concepts of the Delta Sigma Modulator CAM, how it works as an ADC solution, how to use it as a multiplier, how to use it as a divider, and finally how to use it to make an RMS to DC converter.

This application note assumes that the reader is familiar with the AnadigmApex device, its evaluation board and the associated AnadigmDesigner®2 software.

2 Creating The RMS to DC Circuit

2.1 Introduction

The DeltaSigmaMod CAM is a second order switched capacitor Delta Sigma modulator. The CAM is composed of two integrators and a comparator as described in the AnadigmDesigner (AD2) CAM help file.

The CAM converts an analog input waveform to a pulse density modulated (PDM) single bit stream, where the density of ones in the serial digital output is proportional to the input signal value. The bit stream can then be low pass filtered to convert to an analog signal (or the pulses can be counted and processed in a microcontroller or DSP).

2.2 Delta Sigma Waveforms

Figure 1 shows the CAM with simulator signal generator connected to the input and simulator probes connected to input, output and the clock output.

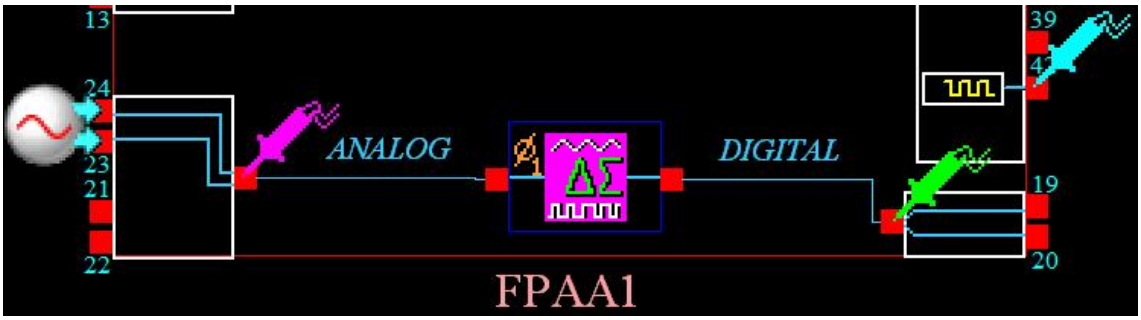

Figure 1: DeltaSigma ADC CAM

A typical O/P waveform from the CAM is shown in figure 2 below (note digital signals are 5V/div, analog signal is 1V/div and the clock is shifted down for clarity). The input is driven with a 3V amplitude, 1KHz sinewave. Note that for clarity, the clock to the DeltaSigma has been slowed right down to 100kHz, and that the PDM waveform would normally contain much higher digital frequencies.

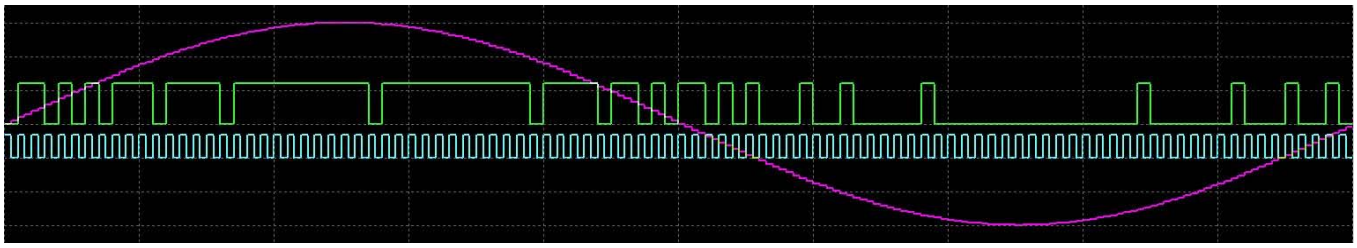

Figure 2: DeltaSigma PDM O/P for 1KHz sinewave, 100kHz clock

Figure 3 shows the output of the same circuit but using a 4MHz clock.

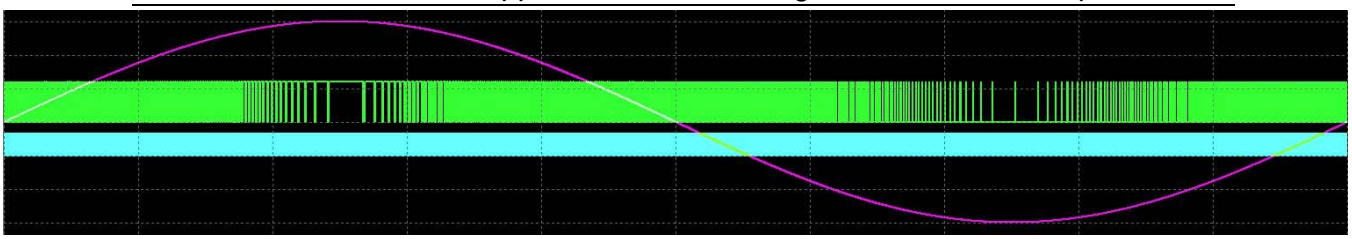

Figure 3: DeltaSigma PDM O/P for 1KHz sinewave, 4MHz clock

2.3 Delta Sigma Multiplier

The output from the DeltaSigma CAM is a single bit stream which can be used to chop (multiply) another waveform. Subsequent low pass filtering yields the analog result. All the CAM's are currently available to achieve this.

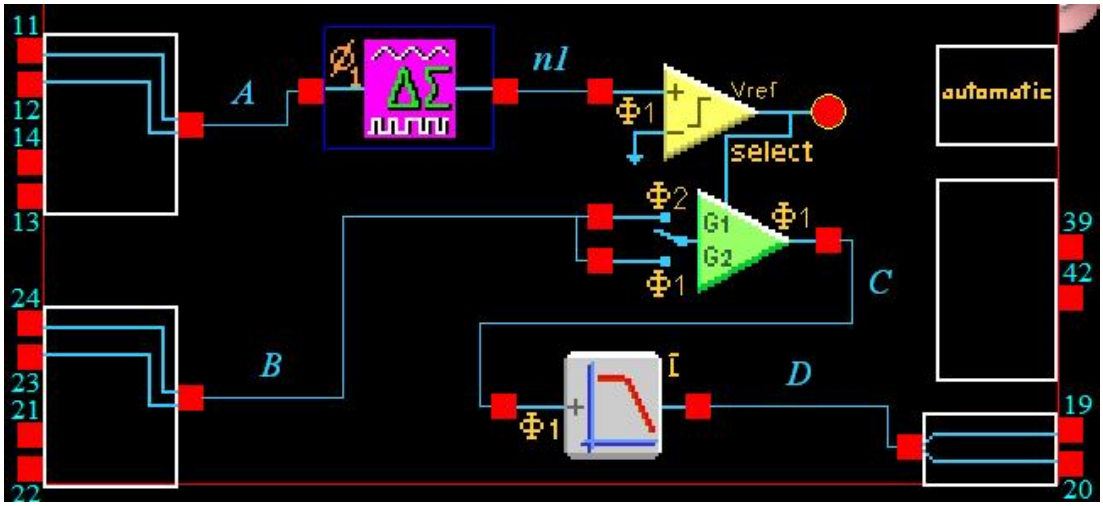

Figure 4: Multipler Circuit

Figure 4 demonstrates just how easy it is to multiply using this technique. Waveform A is converted to a DeltaSigma bit stream, which then chops waveform B using a GainSwitch CAM (gains set to +1 and -1). The resultant waveform C is a pulse density modulated version of the multiplication A x B. This can be filtered in the usual way using a low pass filter CAM to reveal the analog waveform D.

2.4 Delta Sigma Divider

A dividing ADC can be created by simply adjusting the reference voltage to the Delta Sigma. The latest version of the xDeltaSigmaMod CAM in the AD2 customer library (v0.0.9) has been modified to allow access to its reference from within AD2.

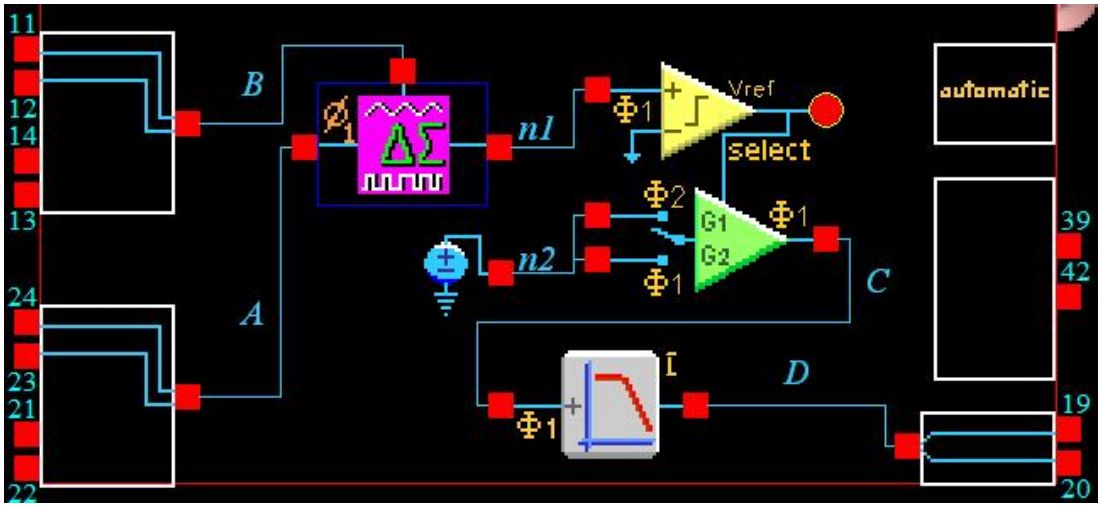

Figure 5: Divider Circuit

The above AD2 snapshot shows signal A being divided by signal B by simply using signal B as the DeltaSigma reference voltage. Node1 (n1) in this diagram is a PDM version of the division, which needs converting back to an analog waveform using an LP filter. However, as the signal is digital the GainSwitch CAM is used first to convert to a friendly +/- 3V for subsequent processing by the FilterBilinear CAM. Signal D is the analog result of A/B.

2.5 RMS to DC Converter

A true RMS converter can be created by using both the Delta Sigma multiplier and divider. Linear Technology market a device based on this approach, LTC1966 (March 2002). A paper by Wey and Huang describes the theory (IEEE Journal of Solid State Circuits, Vol 35, No2, February 2000).

By putting the signal into both inputs of the Delta Sigma multiplier, a square of the input signal is created. The remaining circuit (described later) creates the mean of the square voltage. This is then divided by Vout by connecting Vout back to the Delta Sigma reference input. The formula is shown below…

$$Vout = \frac{\overline{Vin^2}}{Vout} \text{ and hence, } Vout = \sqrt{\overline{Vin^2}} = RMS(Vin)$$

The circuit implementing this function is shown in figure 6.

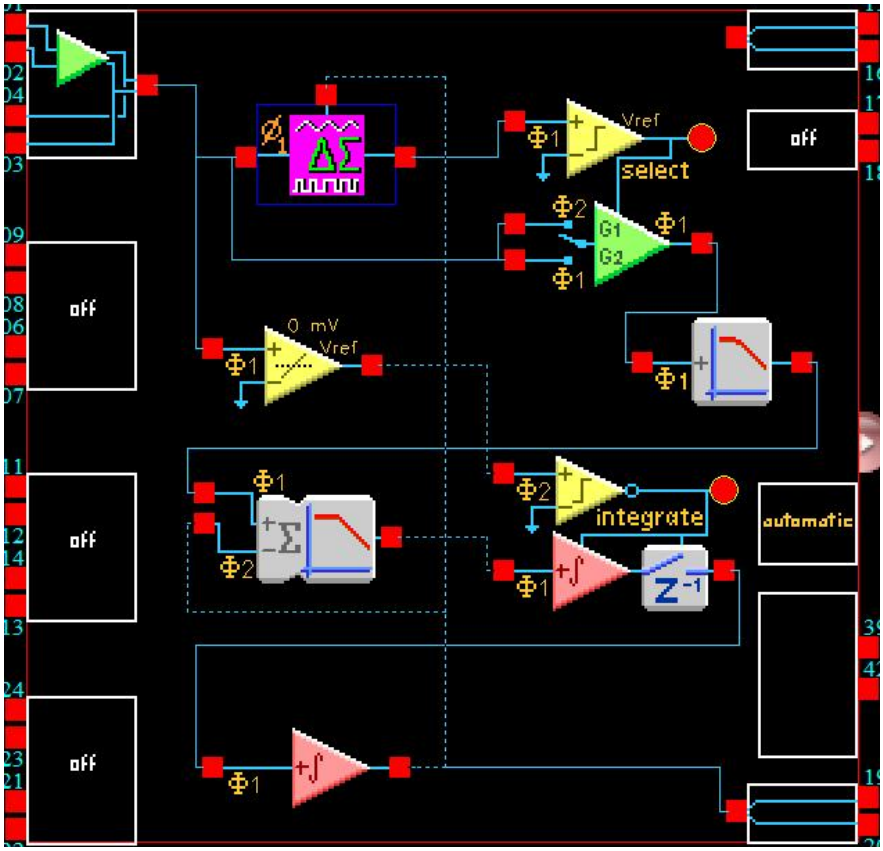

Figure 6: RMS to DC converter

The circuit that follows the square function consists of a Zero Crossing detector CAM, an Integrator Hold CAM or window integrator (sometimes referred to as a boxcar integrator), a Sum Filter CAM and a normal integrator CAM. This entire circuit is designed to average the output of the square function.

Finding the average could be achieved by (severe) low pass filtering, but this circuit is far more sophisticated. It works by subtracting a voltage V from the squared signal and hunting (using the integrator) for the value of V that gives a zero integration of a complete cycle of the offset signal.

The Integrator Hold (window integrator) is triggered by the zero crossing detector and performs the single cycle integration of the offset (by V) version of the squared signal. The single cycle integration is fed into a (slow) integrator, the output of which is subtracted from the squared signal.

The integrator output will settle at a value for which its input is 0V. Its output will then be the offset voltage that achieves zero integration over a cycle i.e. the average of the original square signal.

Finally the average signal is fed back to the reference input of the Delta Sigma CAM which effectively divides it into the input signal.

3 Testing the RMS to DC Circuit

A version of the circuit in figure 6 was created to measure the RMS value of a 60Hz signal. The circuit settings and parameter values were as follows:

xDeltaSigmaMod CAM

Clock = 4MHz

Non-inverting, Phase 1, External Reference On

Reference Divisor Factor = 2.0

GainSwitch CAM

Clock = 4MHz

Signal Ground, Control High, Phase 1, Half Cycle

Gain1 = +1.0, Gain2 = -1.0

FilterBilinear CAM

Clock = 4MHz

Low Pass, Phase 1, Non-inverting, Low Corner Frequency

Corner Frequency = 2.0kHz, Gain = 2.0

ZeroCross CAM

Clock = 3.90625kHz (4MHz / 256)

Signal Ground, Phase 1, Non-inverted, 0mV

SumFilter CAM

Clock = 4MHz

Phase 2, Non-inverting, Non-inverting, Off

Corner Frequency = 4.4kHz, Gain1 = 1.0, Gain2 = 1.0

IntegratorHold CAM

Clock = 7.8125kHz (4MHz / 128)

Non-inverting, Phase 1, Signal Ground, Control Low

Integration Const (1/uS) = 2.04e-005

Integrator CAM

Clock = 7.8125kHz (4MHz / 128)

Non-inverting, Phase 1, No Reset

Integration Const (1/uS) = 7.81e-005

This circuit was tested using a square wave, a sine wave and a triangle wave over a range from 0.1V to 2V amplitude. Figure 7 compares the measurements with the theoretical values. The lines plotting the theoretical values are based on the following formulae:

Triangle Wave: $V_{rms} = V_{peak} / \sqrt{3}$

Sine Wave: $V_{rms} = V_{peak} / \sqrt{2}$

Square Wave: $V_{rms} = V_{peak}$

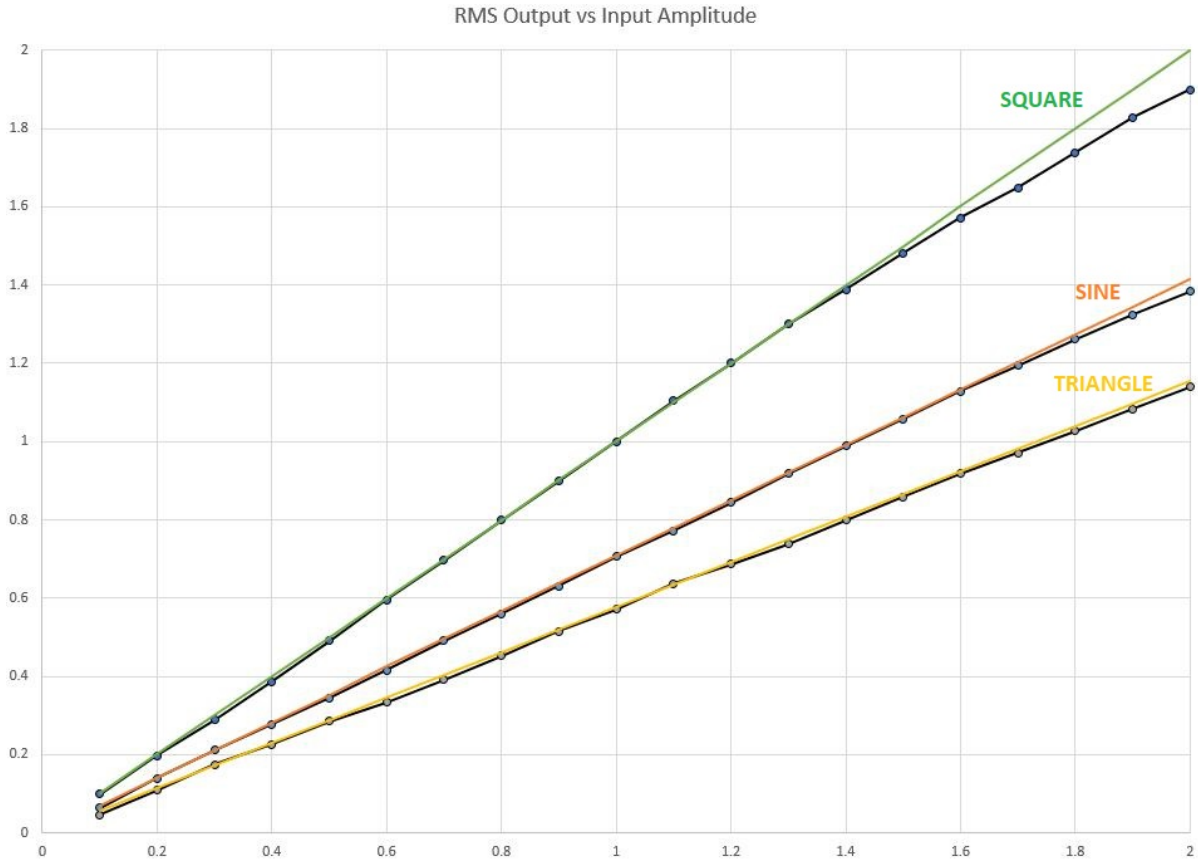

Figure 7: RMS output vs input, measured vs theoretical

The plots in figure 7 show good correlation between measured and theoritcal values for different types of waveform. There is a slight deviation at high inout amplitude (Vpeak > 1.8V) for sinewaves. For square waves the deviation is worse (Vpeak > 1.5V). This deviation is caused by the signal out of the square function hitting the high rail internally and being clipped.

4 Summary

This application note has described the principles of the DeltaSigma CAM, how it can be used to perform multiplication and division, and finally how it can be used to create a true RMS to DC conversion circuit.

The Delta Sigma CAM discussed in this application note is available in the standard library of the latest version of AnadigmDesigner2. The name of the CAM is xDeltaSigmaMod v0.0.9.

If you only have this documentation you can download the supporting .ad2 circuits from here

http://www.anadigm.com/sup_AppNoteLib.asp look for AN231017-U317 A

For more information logon to:
www.anadigm.com