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Introduction

The library of Configurable Analog Modules (CAMs) provided as a part of the AnadigmDesigner^{®2} software allows the analog design to be abstracted at a higher level than transistors or discrete components. Now, designers can define their design in terms of gain stages, integrators, rectifiers etc., wire up the appropriate stages and implement the design in an integrated FPAA.

One of the more popular CAMs available within the AnadigmDesigner^{®2} library of CAMs is the 'Multiplier' CAM that allows the user to multiply two analog signals. This design brief illustrates how such a non-linear function is implemented in the FPAA. It also details some of the more important aspects of obtaining the maximum performance from this CAM.

Overview

The Anadigmvortex device family is based on switched capacitor technology.

This is a linear technology, which says that the transfer function of a given CAM is NOT a function of the signals being applied to it. A gain stage is a good example of a linear system. In a perfectly linear system, doubling the input signal amplitude will exactly double the output signal amplitude. Of course, a practical gain stage will always show some non-linear behavior. Conversely, a non-linear function is one where the transfer function does change with applied signal and a multiplier is a good example of such a circuit.

At the simplest level, the transfer function of a multiplier may be written as:

$$V_{OUT} = \frac{V_{INX} * V_{INY}}{V_{REF}}$$

Here V_{OUT} is the output voltage and the input voltages are V_{INX} and V_{INY} . The voltage V_{REF} must be present to ensure that the equation is dimensionally correct. In the multiplier CAM this voltage is set to be the internal reference voltages, a nominal 3V.

We immediately see that the transfer function from input V_{INX} to output V_{OUT} is controlled by the ratio

$\frac{V_{INY}}{V_{REF}}$. This is clearly a non-linear circuit because the transfer function V_{INX} to V_{OUT} is not fixed, it varies as V_{INY} varies. Similarly, V_{INX} can be regarded as controlling the transfer function from V_{INY} to V_{OUT} .

Multiplication in 1, 2 and 4 quadrants

The output voltage of a multiplier may be sensitive to the polarity of neither, one or both of its inputs.

If the multiplier is insensitive to the polarity of both inputs then the transfer function may be written as:

$$V_{OUT} = \frac{|V_{INX}| * |V_{INY}|}{V_{REF}}$$

The range of values that V_{OUT} may adopt is shown in Figure 1.

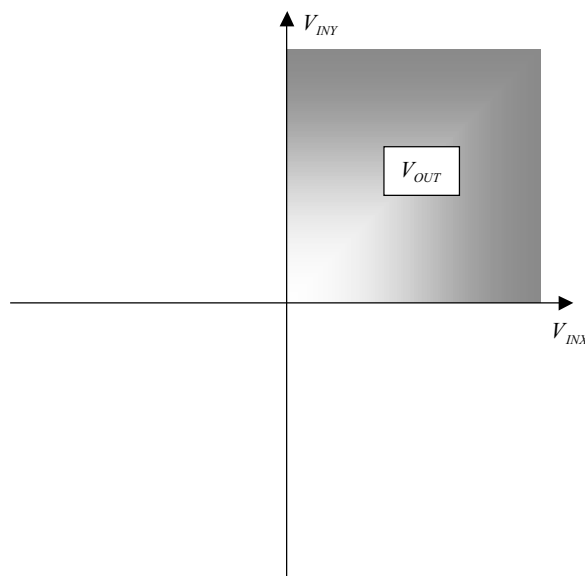


Figure 1: One quadrant multiplication

If the multiplier is sensitive to only one of the input voltage polarities then the transfer function may be written as:

$$V_{OUT} = \frac{|V_{INX}| * V_{INY}}{V_{REF}}$$

Figure 2 shows the corresponding range of output values.

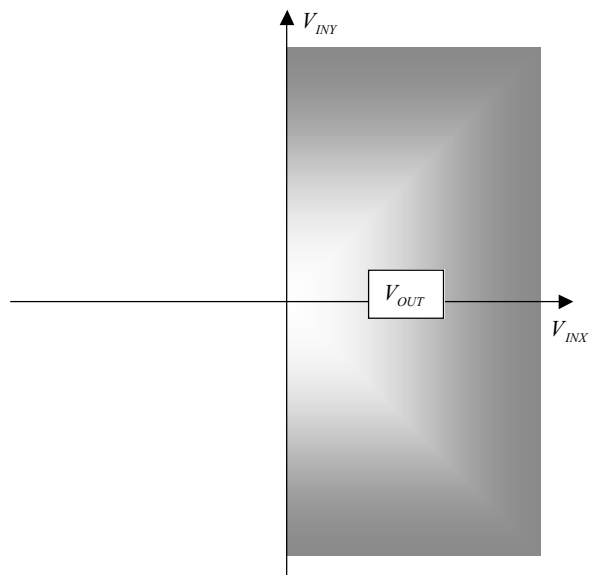


Figure 2: Two quadrant multiplication

Here the output voltage has a polarity which reflects that of V_{INY} but not that of V_{INX} . These inputs can be interchanged, such that,

$$V_{OUT} = \frac{V_{INX} * |V_{INY}|}{V_{REF}}$$

See Figure 3.

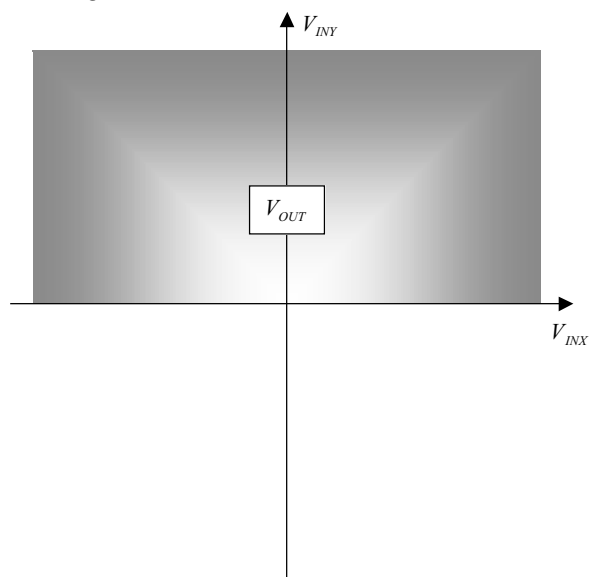


Figure 3: Alternative two quadrant multiplication

When the multiplier is sensitive to both input polarities we have four quadrant multiplication.

$$V_{OUT} = \frac{V_{INX} * V_{INY}}{V_{REF}}$$

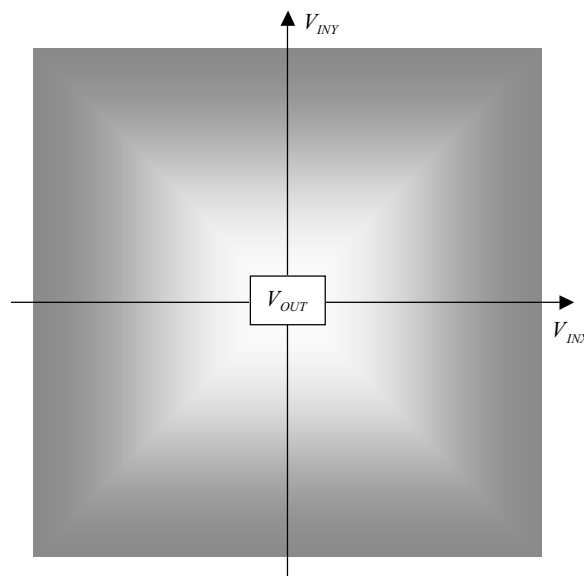


Figure 4: Four quadrant multiplication

The multiplier CAM provided by Anadigm® implements a four quadrant multiplier circuit.

Multiplier CAM internals

A half-cycle offset compensated gain stage is used as the basic circuit element for the multiplier CAM, shown in Figure 5.

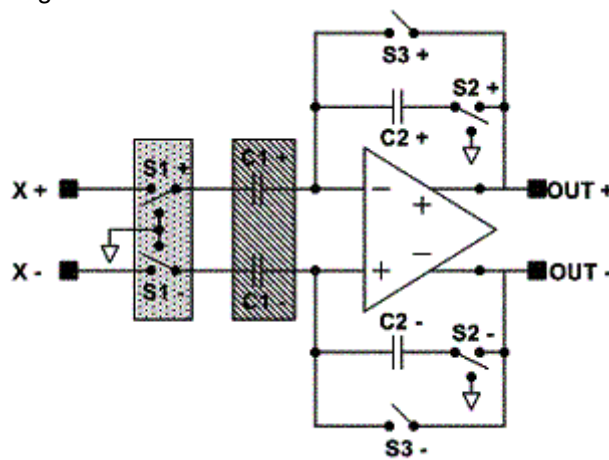


Figure 5: Basic gain stage

This basic gain stage has the linear transfer function

$$V_{OUT} = \frac{C_1}{C_2} * V_{INX}$$

C_1 is the input capacitance and C_2 is the feedback capacitor. The actual values of C_1 and C_2 range from 0 to 255 units and are determined by the data held in RAM local to the gain stage.

The form of the gain stage transfer function makes it clear that the ratio of the two capacitances is the important parameter, and their absolute values are not important to a first order. For example, if C_1 were set to 100 units and C_2 were set to 50 units, then the overall transfer function is seen to be $2x$.

Within this circuit, switches S1 and capacitors C1 sample the input voltage. Switches S2 and capacitors C2 provide a feedback path. Switches S3 are used to reset the circuit, they operate antiphase to switches S2. While the S3 switches are closed, the output of the gain stage is nominally zero.

To a good approximation this circuit is strictly a linear circuit, but the presence of an analog to digital converter (ADC) in the CAM, shown in Figure 6, means we are able to enter the non-linear domain.

The second input to the CAM is V_{INY} (shown as Y+ and Y- in Fig 6). This input is sampled by the ADC within the CAM. The result at the ADC output is an eight bit digital word (D_{OUT}) corresponding to the V_{INY} value. The format of D_{OUT} is sign+magnitude i.e. the polarity of V_{INY} sets the first bit of D_{OUT} and the subsequent seven bits represent the magnitude of V_{INY} relative to the on-chip reference voltages.

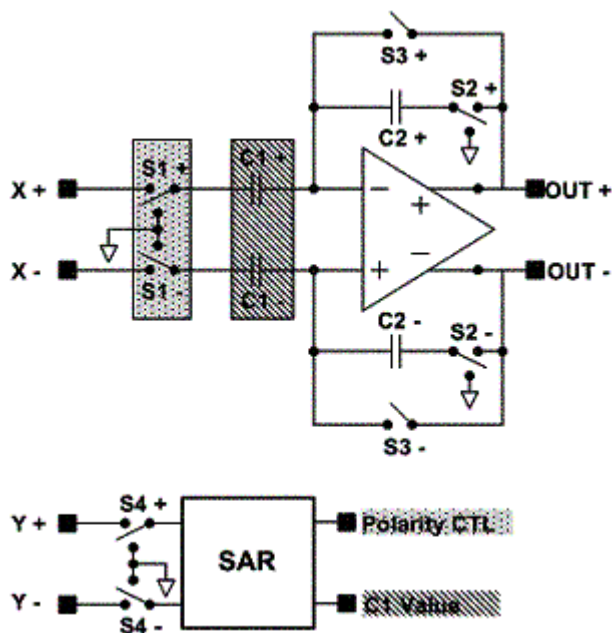


Figure 6: Gain stage plus SAR ADC

For example, if V_{INY} were zero, the first bit would be randomly set (by circuit offsets and noise) to be either 1 or 0 and all subsequent bits would be zero. If V_{INY}

were equal to $+V_{REF}$ then $D_{OUT} = 01111111$ and if $V_{INY} = -V_{REF}$ then $D_{OUT} = 11111111$.

To implement a multiplier, the digital word D_{OUT} is written to the appropriate RAM location such that it sets the value of the input capacitor for C_1 . This means the overall transfer function of Figure 5 can now be written as,

$$V_{OUT} = \frac{\left(\frac{V_{INY}}{V_{REF}} * u \right) * V_{INX}}{C_2},$$

u is the unit capacitance.

Realizing that C_2 may be written as a multiple of the unit capacitance as well, i.e. $C_2 = M * u$ we finally see that,

$$V_{OUT} = \frac{V_{INX} * V_{INY}}{M * V_{REF}}.$$

In the multiplier CAM, C_2 is set to a value such that it is 255 units by default and the digital word D_{OUT} is 255 for a full scale input, meaning in the above equation the two values of 255 can be cancelled and

$$V_{OUT} = \frac{V_{INX} * V_{INY}}{V_{REF}}$$

One drawback of the circuit shown in Figure 6 is that the capacitance written as a representative value of V_{INY} can only ever have a positive value, because there is no physical element to make a negative capacitance.

Such a multiplier would be limited to a two quadrant operation.

This shortcoming is avoided by having the digital word D_{OUT} expressed in "sign + magnitude" format. The sign bit is then used to invert (or not) the phasing of the input switches (S1) while the remaining seven bits of the eight bit word are written to the RAM of C_1 . Thus four quadrant operation is achieved.

Accuracy differences between the two multiplier inputs

The multiplier CAM has two inputs, noted previously as V_{INX} and V_{INY} . The X input is fed directly into the gain stage, but the Y input is fed into the ADC. The Y input is thus 'quantized' to 25mV (i.e. $6V/256$). The resolution of the X input is better than that of the Y input, and the user should bear this in mind when choosing which way around to connect the inputs.

The ADC on the Y inputs limits any incoming signal greater or less than the reference voltages to V_{REF} , as shown in Figure 7.

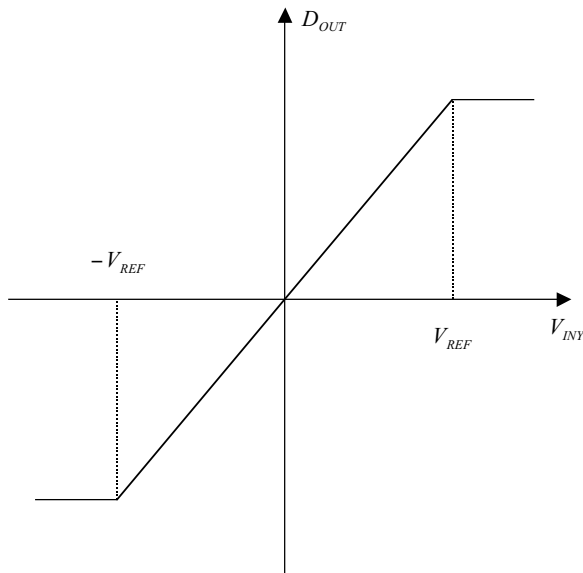


Figure 7: Limiting of output value on the ADC

Sampling differences between the two multiplier inputs.

The multiplier CAM is constructed so that the Y input is sampled on phase 1 of the given clock. The mechanism employed to create a four quadrant multiplier means that the input switches S1 of Figure 5 will sample on either phase 1 or phase 2, determined by the polarity of V_{INY} .

For this reason, the phase of the X input branch cannot be determined in advance and the presence of the $\Delta\phi$ symbol on the multiplier CAM symbol denotes this uncertainty; hence it is important to make sure that the X input to the CAM is valid on both phases of the clock or the input signal may be missed on one of the two possible phases at the X inputs. This is most easily accomplished by using the CAM option to automatically add the appropriate sample and hold to the X inputs.

Timing of the write operation and ADC clocking

The ADC in the multiplier CAM is based on a successive approximation algorithm. It takes nine steps to convert V_{INY} to the appropriate data output D_{OUT} , and a further cycle to write the data to the appropriate RAM location(s). A number of extra clock cycles are usually necessary to allow setting of the analog components before the multiplier takes its next sample of V_{INX} . Consequently, two clocks are required for the multiplier CAM, a relatively slow one for the gain stage and a second faster one (16 times faster) for the SAR ADC.

The 16:1 clock ratio required by the CAM arises from the need to allow time for the SAR ADC to convert V_{INY} to D_{OUT} with some settling time at the end.

The point at which the RAM is updated must be carefully determined within the CAM. When the capacitor C1 has its value altered, some stray charge is usually injected into the gain stage. This is done when S3 is closed and the output of the gain stage is invalid so that the glitch is therefore ignored.

The multiplier gain stage is a circuit which has a valid output for only half the time; it is a half-cycle circuit. Addition of a sample and hold CAM to the multiplier output will produce a full-cycle output if required.

Optional sample-and-hold on the input

To allow an accurate conversion of the Y input, the voltage on this input should not change during the several steps of the conversion. If it does change then an erroneous output may be produced.

To ensure this does not happen, the user must see that either one of two conditions are satisfied.

1. The voltage on V_{INY} changes only slowly relative to the clock rate. It is recommended that no more than 10mV of gradual change should be allowed during a slow clock period. This amounts to $\frac{1}{2}$ LSB of the ADC and will usually not give significant errors.

OR

2. A sample and hold circuit is connected to the V_{INY} terminal to hold the voltage steady during conversion. This sample and hold should be clocked with the slow clock of the multiplier CAM to ensure proper synchronization.

The second option has the advantage of producing better buffering of the Y input and allows the multiplier to be clocked at a higher rate than the suggested defaults.

Example Waveforms

These are provided to illustrate the points made within this design brief and give the user some idea of how to use the multiplier CAM. These waveforms are produced with a sample and hold circuit on the output, so that the half cycle nature of the output is removed, as per Figure 8.

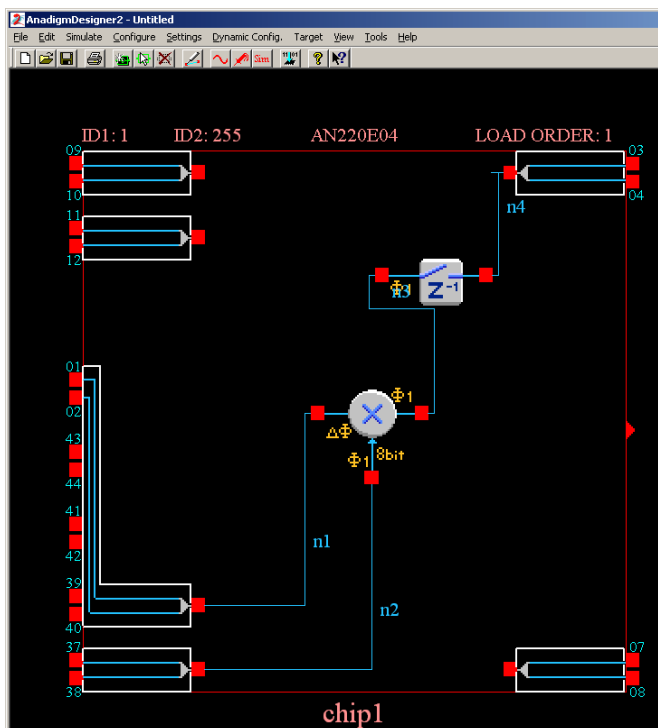


Figure 8: Multiplier CAM with sample and hold added

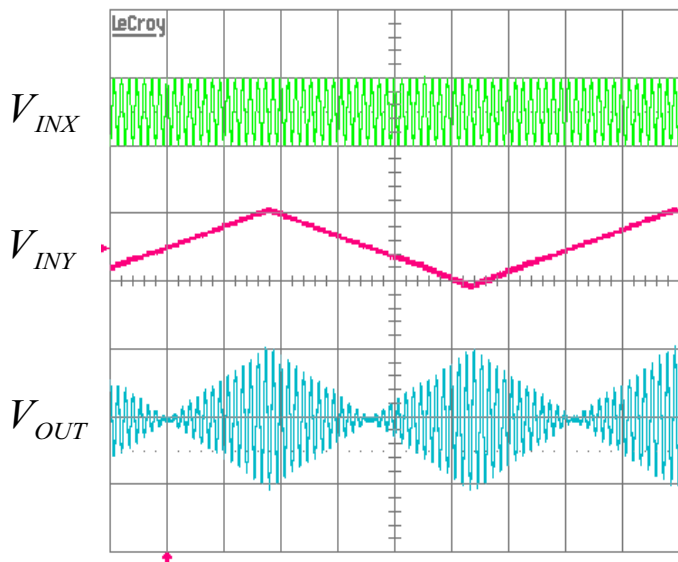


Figure 9: Standard multiplier operation with output sample and hold

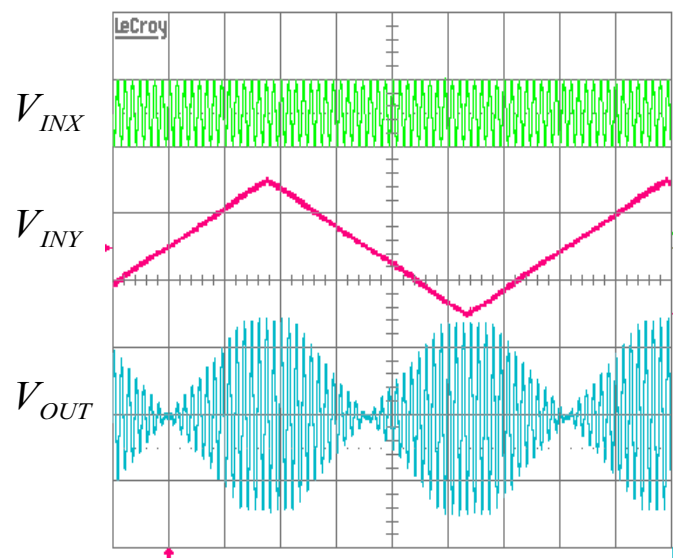


Figure 10: Standard multiplier operation showing input Y saturation, as per Figure 7. Output sample and hold is present.

Removing the sample and hold circuit from the output (Figure 11) allows us to see the half cycle nature of the output, as in Figure 12.

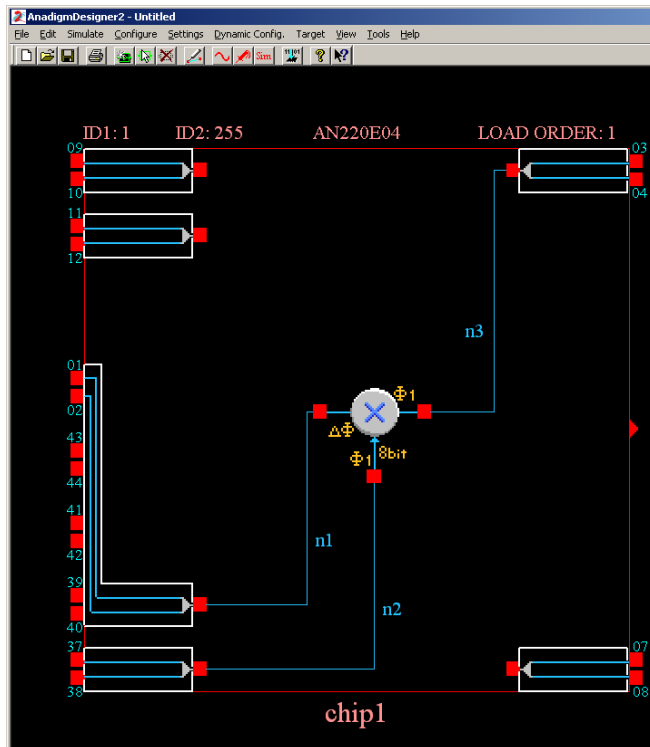


Figure 11: Multiplier CAM WITHOUT sample and hold

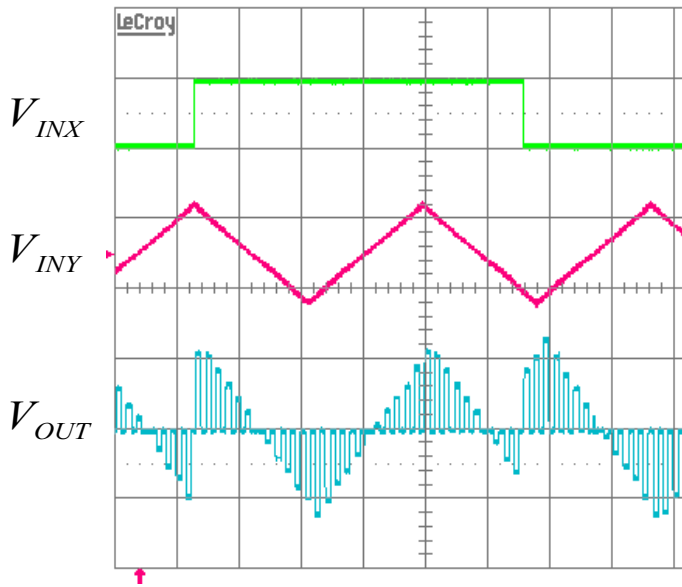


Figure 12: Standard operation without output sample and hold. Half cycle nature of the output is visible.

Figure 13 and 14 show more examples of the multiplier operation.

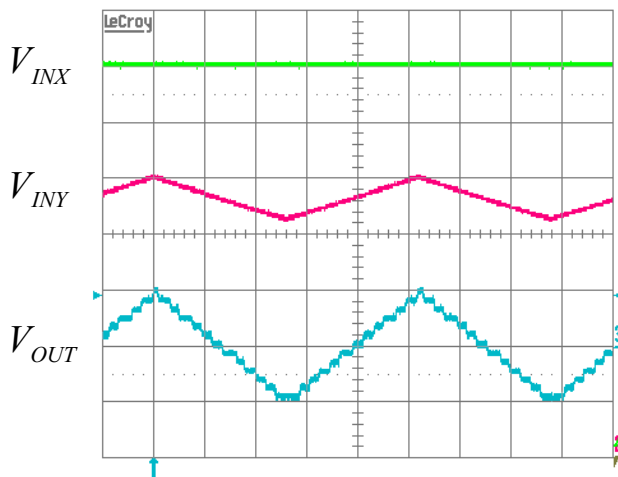


Figure 13: Quantized output due to quantization on Y inputs of multiplier. V_{INX} is a DC input so the transfer function of V_{INY} can be clearly seen. Output sample and hold is used.

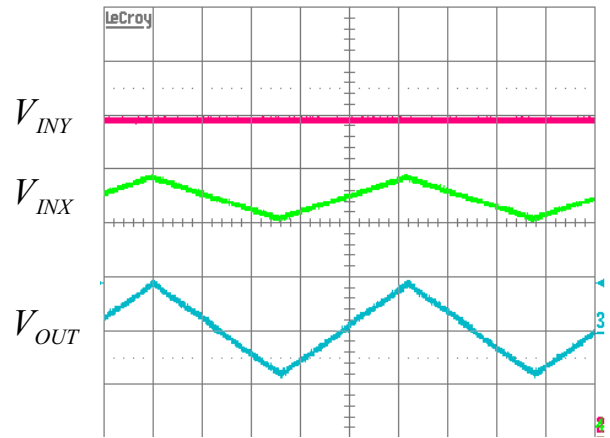


Figure 14: Same circuit as Figure 13 but with inputs swapped over. Better resolution of the X input channel is clear. Output sample and hold is used.

Conclusions

The multiplier CAM has been described in terms of how it works, as well as its internal architecture. It has been shown that the two inputs have the same effect on the output voltage to a first order, but in fact, there are a number of significant differences in practice. The user must consider these to extract the maximum performance from the CAM.

Other variants on the multiplier CAM are being developed within Anadigm® – including a multiplier-filter CAM, and a divider CAM. If you are interested in these CAMs, please contact Anadigm® sales for details.

For more information, please visit Anadigm® at: www.anadigm.com