



# ***Anadigmvortex***

## **Understanding Anadigm<sup>®</sup> Configurable Analog Modules (CAMs)**

- **What is a CAM?**
- **Configuring and Placing CAMs**
- **Other Considerations**
- **CAMs Available in the Anadigm Standard Library**

# What is a Configurable Analog Module (CAM)?

- Circuit building blocks abstracted to a functional level that can be manipulated in AnadigmDesigner<sup>®</sup>2
- A complex circuit can be implemented in a “chip” simply by selecting, configuring, placing and wiring CAMs
- Improved speed and ease of circuit design

# AnadigmDesigner2<sup>®</sup> CAMs

- **Very dynamic, powerful yet easy to use**
  - Multiple circuit topologies – CAM knows how to make what you ask for
  - Dynamic user interface – options and limits can change
    - Allows user to push the limits of the CAM
    - Constrains the user to legal configurations
- **Expanded CAM documentation explains the features**

# Selecting a CAM

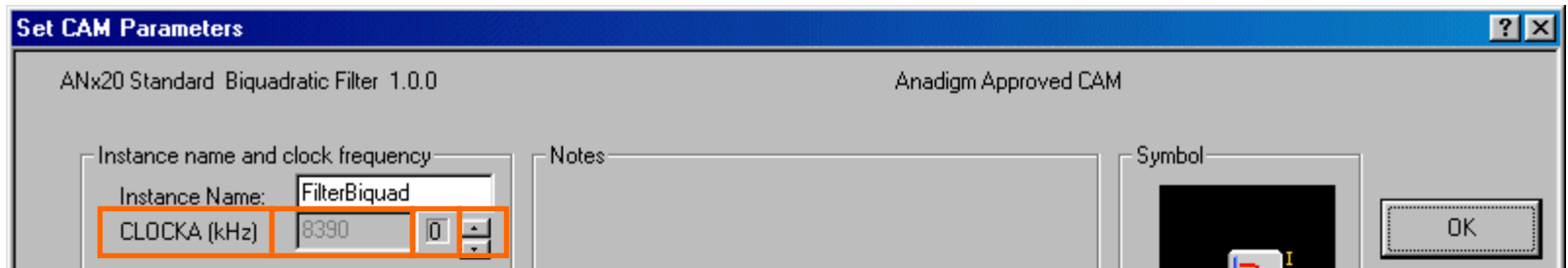
The screenshot shows a 'Select CAM' dialog box with the following elements:

- CAM Libraries:** A list containing 'ANx20 Standard' and 'Tim'. 'ANx20 Standard' is highlighted with an orange box.
- CAMs:** A list of components including 'Comparator - Comparator', 'Differentiator - Inverting Differentiator', 'FilterBilinear - Bilinear Filter', 'FilterBiquad - Biquadratic Filter', 'GainHalf - Half Cycle Inverting Gain Stage with Hold', 'GainHold - Half Cycle Inverting Gain Stage with Hold', 'GainInv - Inverting Gain Stage', 'Hold - Sample and Hold', 'Integrator - Integrator', 'Multiplier - Multiplier', and 'OscillatorSine - Sinewave Oscillator'. 'FilterBiquad - Biquadratic Filter' is highlighted with an orange box.
- CAM:** A text field containing 'FilterBiquad - Biquadratic Filter', with both parts highlighted by orange boxes.
- Buttons:** A 'Display CAM Documentation' button is highlighted with an orange box.

Callouts from a yellow box on the right point to these elements:

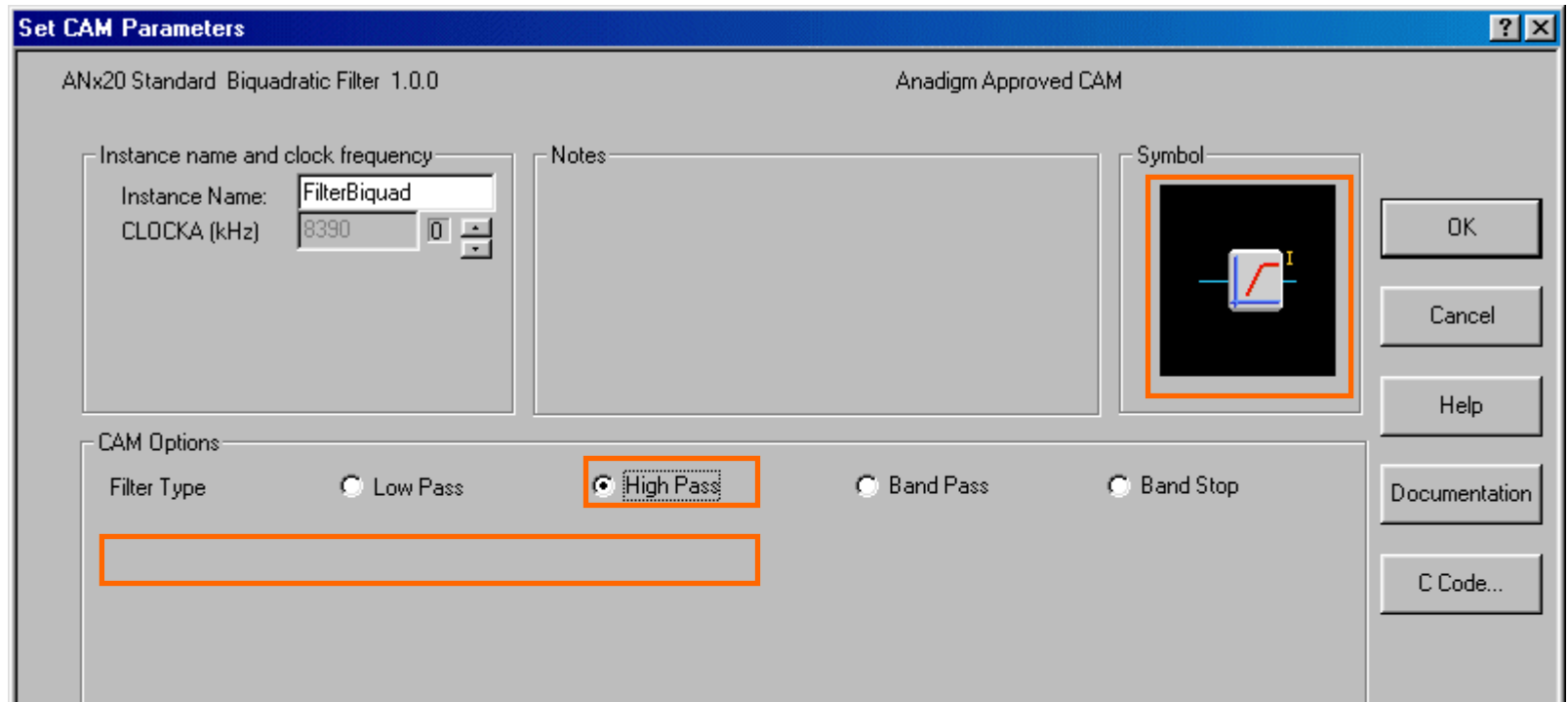
- Library** - ANx20 Standard (points to the highlighted library)
- Name** - FilterBiquad (points to the highlighted component name)
- Description** - Biquadratic Filter (points to the highlighted component description)
- Documentation** (points to the 'Display CAM Documentation' button)

# Configuring the CAM - Clocks



- Set the clock(s)
  - Spinners associate CAM clocks (CLOCKA) with chip clocks (Clock 0) and show the frequency of that chip clock
  - Chip clock frequencies are set in the “Chip Settings” dialog box
- All CAMs in a signal path should use the same chip clock for the analog clock (CAM CLOCKA)
- Some CAM parameters are clock dependent (filter corner frequency)
  - These CAMs should be reconfigured if the clock frequencies are changed
- CAMs with multiple clocks contain instructions about their relation

# Configuring the CAM - Options



- CAM Options
  - Option settings control circuit configuration. This is reflected in the symbol. Options and parameters may also change
  - Options may be gray due to incompatible combinations or unavailable resources

# Configuring the CAM - Parameters

ANx20 Standard Biquadratic Filter 1.0.0

Instance name and clock frequency

Instance Name: FilterBiquad

CLOCKA (kHz): 8390

Notes

CAM Options

Filter Type:  Low Pass  High Pass

CAM Parameters

Parameter:	Value:	Limits:	Realized
Corner Frequency [kHz]	83.9	16.8 To 839	83.9
Gain	1	0.0100 To 8.00	1.00
Quality Factor	0.707	0.0100 To 100	0.706

Parameter Names

- May include units

Desired Value

- Entered by the user

Parameter Limits

- Values will be restricted

Realized Value

- What was possible for this combination of desired values



# Parameters - Quantization and Error

Parameter:	Value:	Limits:	Realized
Gain 1 (UpperInput)	1	0.0100 To 6.55	1.00
Gain 2 (LowerInput)	0.0257	0.0100 To 100	0.0258

- Realized values show the implementation of the parameter based on ratios of programmable capacitor banks which are **quantized**

$$\frac{6 \text{ unit caps}}{233 \text{ unit caps}} = 0.02575$$

- Actual measured values can have **error** in addition to the quantization of the realized value

$$Gain_{Realized} = 0.02575$$

$$Gain_{Measured} = 0.0259 \Rightarrow 0.6 \% \text{ error}$$

# Parameters - Interrelation

Parameter:	Value:	Limits:	Realized
Gain 1 (UpperInput)	6	0.0100 To 6.55	6.00
Gain 2 (LowerInput)	0.0257	0.0235 To 100	0.0256

$$\frac{234 \text{ unit caps}}{39 \text{ unit caps}} = 6.0 \quad \frac{1 \text{ unit caps}}{39 \text{ unit caps}} = 0.02564$$

- Realized values are based on the combination of capacitor ratios. Changing one desired value can change multiple realized values.

- Limits are dynamic. Changing desired values can also change the limits.
  - If Gain 1 = 6.0  
Gain 2 cannot be less than 0.0235
  - If Gain 2 = .0257  
Gain 1 cannot be greater than 6.55

# Configuring the CAM - LUT

Set CAM Parameters

ANx20 Standard User-defined Voltage Transfer Function 1.0.0

Anadigm Approved CAM

Instance name and clock frequency

Instance Name: TransferFunction

CLOCKA (kHz): 1048.75

CLOCKB (kHz): 16780

Notes: Enter voltage transfer function profile by pressing the Lookup Table button.

Symbol

OK

Cancel

Help

Documentation

C Code...

Lookup Table

Dialog

Voltage Transfer Function

Limits = -4 to 4

Vin	Value	Realized
$X < -2.977$	0.000000	0.000000
$-2.977 < X < -2.953$	0.000000	0.000000
$-2.953 < X < -2.930$	0.000000	0.000000
$-2.930 < X < -2.906$	0.000000	0.000000
$-2.906 < X < -2.883$	0.000000	0.000000
$-2.883 < X < -2.859$	0.000000	0.000000
$-2.859 < X < -2.836$	0.000000	0.000000
$-2.836 < X < -2.813$	0.000000	0.000000
$-2.813 < X < -2.789$	0.000000	0.000000
$-2.789 < X < -2.766$	0.000000	0.000000
$-2.766 < X < -2.742$	3.210000	3.201681
$-2.742 < X < -2.719$	0.000000	0.000000
$-2.719 < X < -2.695$	0.000000	0.000000

- Parameter entry to set output voltages
  - Limits
  - Input voltage range that will trigger this output
  - Desired value
  - Realized value

# Configuring the CAM - Finishing

**Set CAM Parameters** [?] [X]

ANx20 Standard User-defined Voltage Transfer Function 1.0.0      Anadigm Approved CAM

Instance name and clock frequency

Instance Name:


CLOCKA (kHz)

CLOCKB (kHz)

Notes

Enter voltage transfer function profile by pressing the Lookup Table button.

Symbol



OK

Cancel

Help

Documentation

Read any notes for help with configuration

- Documentation
  - Online help about this CAM
- Cancel
  - Discard all changes
- OK
  - Accept all changes

CAM Parameters

Parameter:	Value:
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# Online CAM Documentation

**Half Cycle Gain Stage**

**Hardware Compatibility**  
This CAM is compatible with the following chip types:  
anADIGM-AN002001

The Gain Stage is a half cycle gain stage. The input output is scaled by the value of the programmable gain, and the CAM may be either inverting or non-inverting. The output has amplifier input offset compensation during its valid output phase.

**Related CAMs**  
The Gainable CAM creates a full cycle inverting gain stage. This gain stage has continuous input and continuous output that is always valid.  
The Gainable CAM creates a half cycle inverting gain stage with output hold. It has a sampled input and an output that is valid during half phase.  
The output has amplifier input offset compensation during a single output phase. The upper gain limit may be higher than that of a Gainable CAM.

**CAM Options: Polarity**  
This is the option for a gain stage with input phase 1. Other variants are available.  
Resistoring: The half cycle output is delayed by one phase (one half of a clock period) in the non-inverting version.  
Switching: This is the option for a gain stage with input phase 1. Other variants are available.  
CAM Options: Input Sampling  
This is the option for a non-inverting gain stage. Other variants are available.  
Phase 1: This version should be connected to sample a signal in either output phase 1 or continuously valid.  
Phase 2: This version should be connected to sample a signal in either output phase 2 or continuously valid.

**CAM Parameters:**

Gain	0.00 - 0.10 (V <sub>in</sub> = 0.00V)	0.10 - 0.15 (V <sub>in</sub> = 0.00V)	0.15 - 0.20 (V <sub>in</sub> = 0.00V)	0.20 - 0.25 (V <sub>in</sub> = 0.00V)	0.25 - 0.30 (V <sub>in</sub> = 0.00V)	0.30 - 0.35 (V <sub>in</sub> = 0.00V)	0.35 - 0.40 (V <sub>in</sub> = 0.00V)	0.40 - 0.45 (V <sub>in</sub> = 0.00V)	0.45 - 0.50 (V <sub>in</sub> = 0.00V)
	0.00	0.10	0.15	0.20	0.25	0.30	0.35	0.40	0.45

**Circuit Diagram and Design Equations:**  
The transfer function for the circuit is:  
$$\frac{V_{out}}{V_{in}} = -\frac{C_2}{C_1}$$
  
The circuit realizing this CAM is shown in the figure at right.  
The capacitor values are chosen based on the best values of the capacitors satisfying the following relations:  
$$C_2 = \frac{C_1}{10}$$

Switch phasing is dependent on CAM option. Switch phasing for the primary connections is given in the following table. The primary switch is closed on the phase indicated. Switch phasing for secondary connections is appropriate in the complement of the primary phasing. Secondary connections to output ground on the opposite phase from the primary switch.

**Switch Phasing:**

Polarity	Input Sampling	S1	S2	S3
Inverting	Phase 1	0	1	0
Inverting	Phase 2	1	0	0
Inverting	Phase 1	0	0	1
Inverting	Phase 2	1	1	0
Non-Inverting	Phase 1	1	0	0
Non-Inverting	Phase 2	0	1	0
Non-Inverting	Phase 1	0	0	1
Non-Inverting	Phase 2	1	1	0

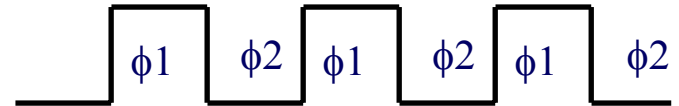
**Output Characteristics**  
The inverting version of this CAM does not have additional phase delay due to sampling as the half cycle output is available during the input sampling phase. The non-inverting version of this CAM exhibits one phase time half of a clock period of delay. Therefore the half cycle output is available one phase time half of a clock period after the input was sampled. The appropriate phase for the input and output is shown in the circuit diagram.  
This CAM is bufferless with the output phase as a function of polarity and input sampling as related. The output will be equal ground depending on the other phase. The maximum output voltage CAM is only valid during one phase.

- Anadigm approved CAMs contain information about CAM construction and proper usage
  - Details about each CAM option
  - Details about each CAM parameter
  - Design Equations
  - Circuit Diagrams
  - Switch Phasing
  - Output Characteristics
- Some include additional design notes with information about special features of that CAM

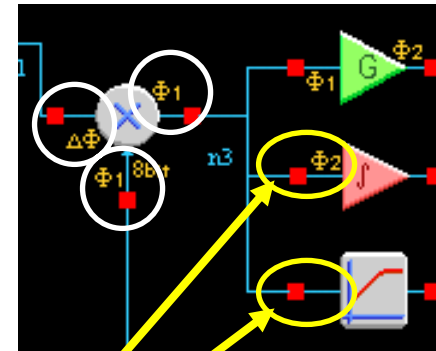
# Placing and Wiring CAMs

- **Place the CAM within the chip borders**
  - Green warning marker indicates the CAM cannot be dropped on top of something
  - Red warning marker indicates that available resources are not sufficient to implement the CAM
- **Draw wires between the CAM contacts**
  - Only legal connections will be allowed
- **Chips can be connected for simulation**

# Other Considerations – Clock Phases



- Each clock has two non-overlapping phases
- Phase symbol on a CAM input shows an input that samples only on that phase
  - $\Delta\phi$  indicates that the sampling phase changes during operation
- Phase symbol on a CAM output shows the output should be sampled on that phase



- **Warning:** a phased output can be safely connected only to a similarly phased input
- Always see the CAM documentation for details on input/output characteristics

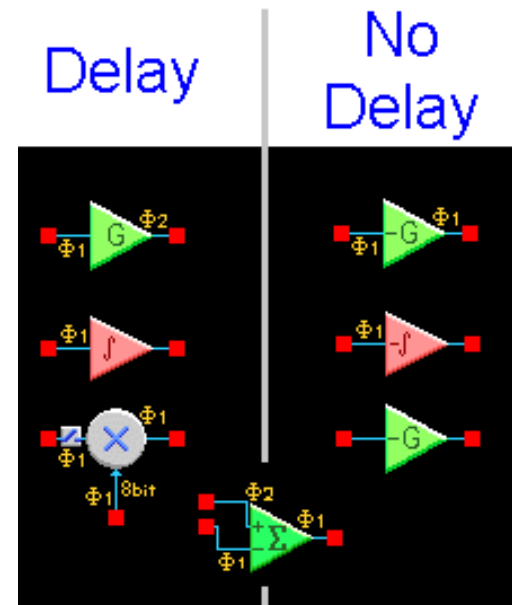
# Other Considerations – Clock Delay

- CAMs may have signal delay due to the timing of clocked switches. This is not the same as filter phase delay.
- Clock delay can often be neglected if the clock frequency is adequately higher than the signal frequency

Example – 10 kHz signal CAM  
has half clock cycle delay

- With 50 kHz clock  
36 degree delay (possibly significant)
- With 1 MHz clock  
1.8 degree delay (probably negligible)

- Clock delay is not shown by symbol alone
- Always see the CAM documentation for details on input/output characteristics





## .cam File




- Primary CAM file
- ASCII based
- Read directly by AnadigmDesigner2
- Strictly formatted, keyword driven with very little error checking

Name, Version, User Interface  
Control, Circuit Definition,  
Parameter Calculation, Symbol,  
Simulation equations, CCODE, etc.

## .chm File

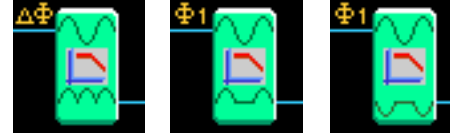
- CAM Documentation or Help file
- Compiled HTML
- Referenced and displayed by AnadigmDesigner™

# Standard Library CAMs – Gain Stages

- **GainHalf** 
  - Half-cycle
- **GainHold** 
  - Inverting only
- **GainInv** 
  - Continuous Time

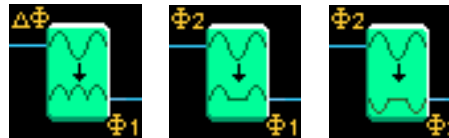
# Standard Library CAMs – Rectifiers

- **RectifierFilter**



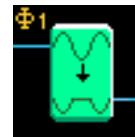
- Full Wave/Half Wave
- Inverting/non-inverting

- **RectifierHalf**



- Full Wave/Half Wave
- Inverting/non-inverting

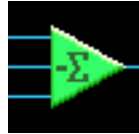
- **RectifierHold**



- Half Wave Inverting only

# Standard Library CAMs – Summing

- **SumInv**



- Up to three inputs

- **SumDiff (SumHalf)**



- Up to four inputs
- Add or subtract since input branches can be inverting or non-inverting

# Standard Library CAMs – Filters

- **FilterBilinear – One pole**



- Low Pass/High Pass/All Pass

- **FilterBiquad – Two poles**



- Low Pass/High Pass/Band Pass/Band Stop
- Automatically chooses from multiple circuit topologies



**Some other CAMs use a low pass bilinear filter as part of another function (RectifierFilter)**

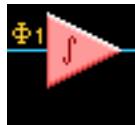
# Standard Library CAMs – Math

- **Differentiator**

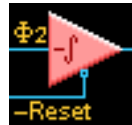


- Output voltage slews – see documentation

- **Integrator**



- Optional reset

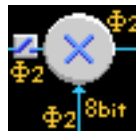


# Standard Library CAMs – Multiplier

- **Multiplier**



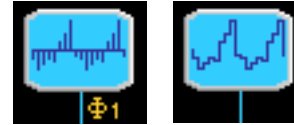
- Uses SAR (Input Y is quantized)
- Subject to internal reference voltage error
- Optional sample and hold on input X to equalize sampling time of two inputs (uses chip resources)



# Standard Library CAMs – LUT

- **PeriodicWave**

- Half-cycle/Output Hold



- Uses LUT to generate a user-defined periodic sequence of output voltages
- Documentation has help with loading the LUT

- **TransferFunction**

- Half-cycle/Output Hold



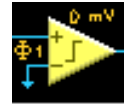
- Uses the SAR and LUT to perform A/D conversion on the input and generate the appropriate user-defined output voltage



# Standard Library CAMs - Other

- **Comparator**

- Single/Dual Input
- Variable Reference



- **Hold – Sample and hold**



- **OscillatorSine**



- Subject to internal reference voltage error

- **Voltage (+/- 3 VDC)**



- Subject to internal reference voltage error