RangeMaster2 Datasheet

Programmable Analog Signal Processor for a Universal RFID tag reader system

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PRODUCT OVERVIEW

The RangeMaster2 solution is based on the 3rd generation programmable Analog Signal Processing technology developed by Anadigm.

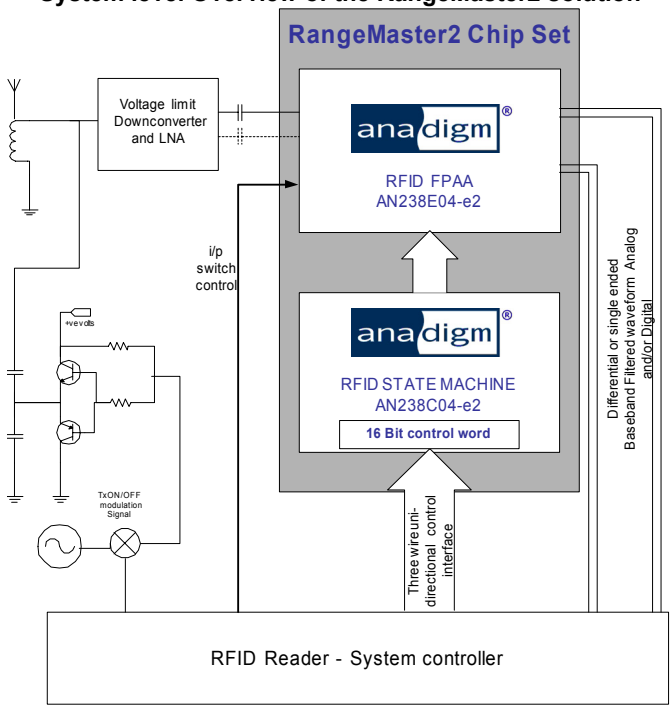
It allows for the development of a universal RFID tag reader that can read multiple tag types.

By allowing standardization around a single PCB to support multiple end products and markets, the RangeMaster2 promises to lower total cost of ownership and simplify product development

This solution enables customized signal processing using the system host controller. Some of the options that are user customizable are:

1. The signal processing circuit implemented in the RFID dpASP – choose between twin or triple band-pass filter, Class0 or a single wide-pass filter.
2. The background frequency that is filtered out – select from 3 predefined values.
3. The gain and balance of the overall analog circuit – optimize the range and sensitivity of the reader
4. The upper and the lower sub carrier frequency – select from 15 predefined values
5. Differential or single-ended analog signal paths.
6. Digital and/or analog output

System level Overview of the RangeMaster2 solution



UHF CARD READER

PRODUCT FEATURES

- Complete baseband Solution for Universal RFID Reader
- Full support for EPC Global Gen 1/Gen 2 (Class 0,1,2) and ISO18000-6 protocols
- User customizable signal processing – Choice of four different sub-carrier - baseband processing circuits
- Selectable sub-carrier frequency or frequency pairs
- Read range and sensitivity optimization with variable gain and balance
- Ability to calibrate reader to filter out background interference (i.e. fluorescent lighting)
- Standby Mode for minimum power consumption
- Two-chip solution
- Supply voltage: 3.3v
- RFID dpASP Package: 44-pin QFN (7x7x0.9mm)
  - Pad pitch 0.5mm
- RFID State Machine:20-pin SSOP(5.3x7.2x1.75mm)
  - Lead pitch 0.8mm

BENEFITS

- Easy to use pre-defined Analog signal conditioning path.
- Design and maintain ONE reader that can be customized to read different tag types, with different modulation schemes and frequencies
- Dynamically change the filter frequencies and circuit architecture
- Supports transmit path signal suppression, avoid receiver saturation recovery time.
- Adjust the gain of the analog signal path to optimize for read range
- Standardize around a single PCB to support multiple end products and markets
- Calibrate the reader at customer site – to account for background interference
- Reduce the total number of system components and lower bill of materials cost

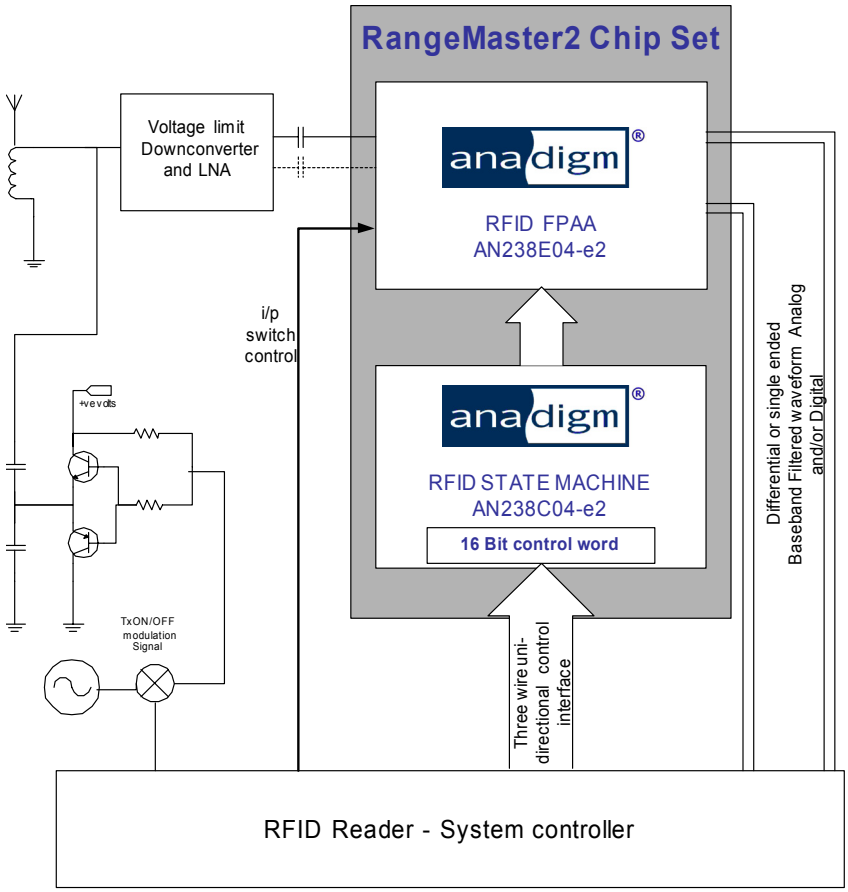
ORDERING CODE (This chipset is only available in RoHS compliant material set)

The RangeMaster2 Chip set is sold in pairs of devices either in trays and tubes or in Tape And Reel format. Both devices are provided in lead-free, RoHS compliant material. Lead finish Matt tin (Sn) and Matt tin & copper (SnCu).

- AN238K04-SETTY (chipset pair) consists of :-
  - AN238E04-e2-QFNTY (260/Tray,1300/box)
  - AN238C04-e2-SSOTY (66/Tube, 1300/box)
- RangeMaster2 Evaluation board
  - AN238K04-e2-EVAL2
- AN238K04-SETTR (chipset pair) consists of :-
  - AN238E04-e2-QFNTR (1000/Tape & Reel)
  - AN238C04-e2-SSOTR (1000/Tape & Reel)
- RangeMaster2 (chipset pair) Single Pack Samples
  - AN238K04-e2-SETSP

[*For more detailed information on the features of the RangeMaster2 solution, please contact Anadigm Technical Support, support@anadigm.com*]

1. INTRODUCTION - ANALOG SIGNAL PROCESSING



UHF CARD READER

The RangeMaster2 chip set consists of an RFID dpASP integrated circuit (dynamically programmable Analog Signal Processor) and an RFID State Machine Circuit, together the devices offer sufficient flexibility to cover the Analog sub-carrier signal conditioning for a universal RFID reader unit.

RFID dpASP, is a variant of Anadigm's dynamically configurable Analog Signal Processor, SRAM based programmable Analog circuitry. The RFID State Machine is a controller with the knowledge embedded to allow it to re-configure the RFID dpASP with one of four base circuits, each of which has multiple programmable attributes, the user is exposed to the control of these circuit variations via a simple 16 bit control word within the RFID State Machine, which is written and re-written via a 3 wire (SPI compatible) interface. The analog input signal to the RFID dpASP is ideally an ac coupled differential signal, however an ac coupled single ended signal can also be accommodated.
The RangeMaster2 solution lets users select between four analog signal processing circuits:

- the universal baseband processing circuit, (see section 1.1, Fig 1) and
- the EPC Gen2 or twin baseband processing circuit (see section 1.2, Fig 2)
- the triple baseband processing circuit (see section 1.3, Fig 3)
- the Class0 baseband signal processing circuit (see section 1.4, Fig 4)

The signal path within the RFID dpASP is fully differential, both gain and filter corner frequencies are variable in each circuit (except the Class0 circuit). Within the "RFID_wide" signal path there is an additional optional narrowband Notch filter with three preset center frequencies. Within the "RFID_twin" and "RFID_triple" signal path the mixer element has variable gain in each input branch, three preset gain boosts are preconfigured for the lower frequency signal path (0, 3 and 6dB), this allows for signal amplitude balancing before the summing stage.
The Class0 circuit offers fixed filter corner frequencies and fixed gain.
Both signal paths offer a fully differential analog output signal, this can also be used single-ended in which case the signal has half the amplitude and a +1.5 volt dc bias. Similarly both circuits paths offer a digital output, this is the result of feeding the analog signal through a comparator with differential hysterisis thresholds set to +/-570mV, the digital output is available as a complimentary pair (inverted or non-inverted).

The RangeMaster2 output signal requires the final stage of decoding to be performed in a "system controller" unit, extracting the data bit stream. Decoding of the FSK (or other encoding) from the digital output is a simple matter of timing sequential edges, final decode of the Analog bit stream can be as simple as a comparator or much more sophisticated eg include statistical and amplitude functions.

1.1 Universal Baseband Processing Circuit (RFID_wide).

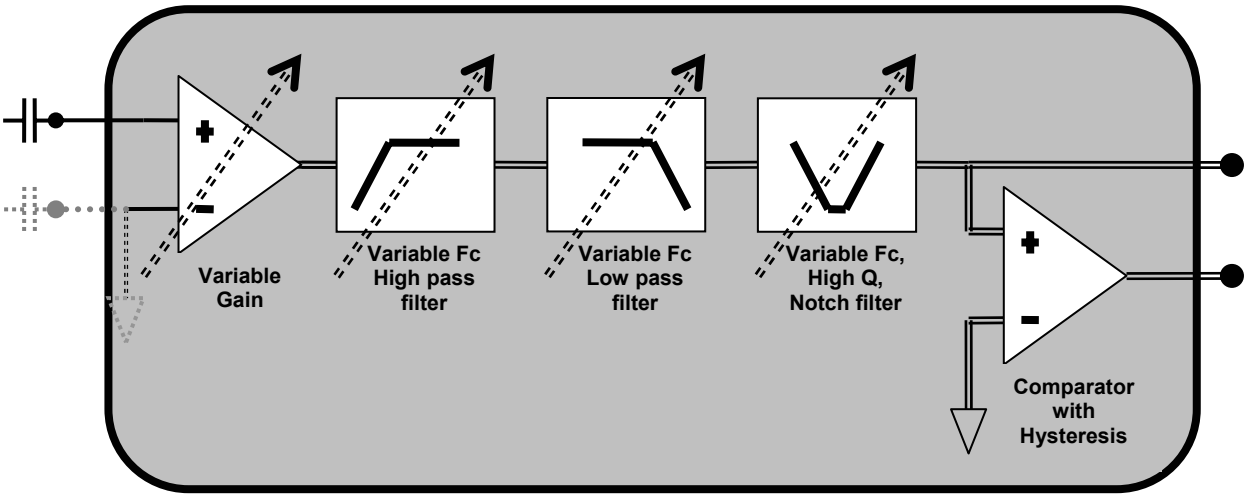


Fig 1: Universal analog baseband processing circuit

The universal circuit enables the extraction of all data frequencies (DC to 848kHz).
It also features a user selectable notch filter for rejecting background interference (i.e. fluorescent lighting).

Gain stage	Control word G1 to G4	Gain (dB)	Gain	Tolerance	Comment
	0000	N/A	N/A	N/A	Only used for Standby.
	0001	0	1.00	0.10%	Inverting differential gain stage,
	0010	6	2.00	0.18%	
	0011	12	3.98	0.50%	
	0100	18	7.94	1.45%	
	0101	24	15.85	1.89%	
	0110	30	31.62	3.03%	
	0111	N/A	N/A	N/A	Not used
	Upper 8 nibbles	N/A	N/A	N/A	Not used in this circuit , there is no Summing stage to adjust.

Highpass filter	Fc (-3dB point, kHz)	Tolerance	Comment
Control word bits LF1 to LF4	2, 4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 424	Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1 Quality factor = 0.707 Inverting architecture

Lowpass filter	Fc (-3dB point, kHz)	Tolerance	Comment
Control word bits HF1 to HF4	4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 640, 848.	Better than 1%	2nd Order Biquadratic, Butterworth approximation Lowpass Gain=1 Quality factor = 0.707 Inverting architecture

Notch filter		Fc (Notch center point, kHz)	Tolerance	Comment
Control word bits A3 and A4	00	Notch filter is removed from the signal path		2nd Order Biquadratic Quality Factor = 20 Gain's 1.00. Inverting architecture
	01	50	Better than 1%	
	10	52		
	11	54		

Comparator	Hysterisis	570mV	10%	Complimentary outputs available

See graphical data for filter response details (Next pages).

The Control word as it applies to Circuit 1, RFID_wide.

ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)

Select circuit		Notch filter center frequency		Gain control				Lower subcarrier frequency (this sets lower bandpass or Highpass filter)				Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														LSB
A1	**A2**	**A3**	**A4**	**G1**	**G2**	**G3**	**G4**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
0	**0**	B1,B2	Freq (kHz)	G1,G2,G3,G4	Bulk Gain	LF gain	HF gain	LF1,LF2, LF3,LF4		Freq (KHz)		HF1,HF2, HF3.HF4		Freq (KHz)	
00 = Universal (WIDE) bandpass		00	*Note4*	0000	*Note5*	*Note5*	*Note5*	0000		2		0000		4	
		01	**50.0**	**0001**	**0dB**	+0dB	+0dB	0001		4		0001		8	
		10	52.0	0010	+6dB	+0dB	+0dB	0010		8		0010		16	
		11	54.0	0011	+12dB	+0dB	+0dB	0011		16		0011		20	
				0100	+18dB	+0dB	+0dB	0100		20		0100		32	
				0101	+24dB	+0dB	+0dB	0101		32		0101		40	
				0110	+30dB	+0dB	+0dB	**0110**		**40**		0110		64	
				0111		Not used		0111		64		0111		80	
				1000				1000		80		1000		106	
				1001				1001		106		1001		128	
				1010				1010		128		1010		160	
				1011		Not used		1011		160		1011		212	
				1100				1100		212		1100		256	
				1101				1101		256		**1101**		**320**	
				1110				1110		320		1110		640	
				1111				1111		424		1111		848	

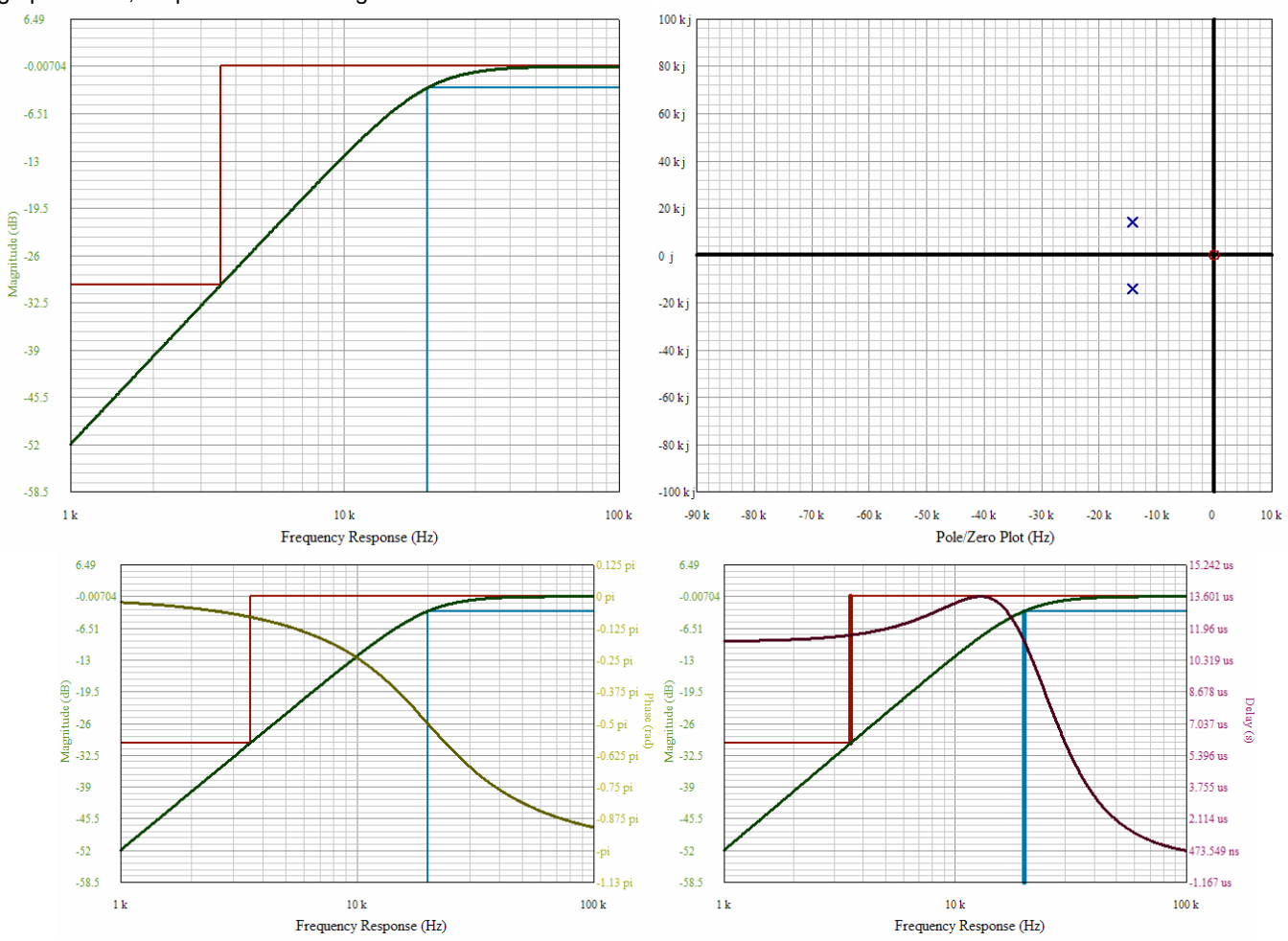
Notes

1) bold - Bold text indicates the default circuit, the RangeMaster chipset will start-up with this circuit
the chipset starts up with this circuit after power up or reset,
but, if the chipset is awakened from sleep (by a dummy config) then it remembers the circuit it had before it went to sleep.

4) The notch filter is removed from the signal path. Notch filter is only used in the Universal WIDE filter

5) Control word 0000000000000000(binary), 0x00, 0x00 (Hex) sets the chipset into standby (low power mode)

High pass filter, Chipset default setting 20 kHz.



At 20kHz, (default setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	20kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	3.55 kHz
Actual Corner Frequency	19.98kHz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (88752.2-88752.2j))·(S + (88752.2+88752.2j))]		

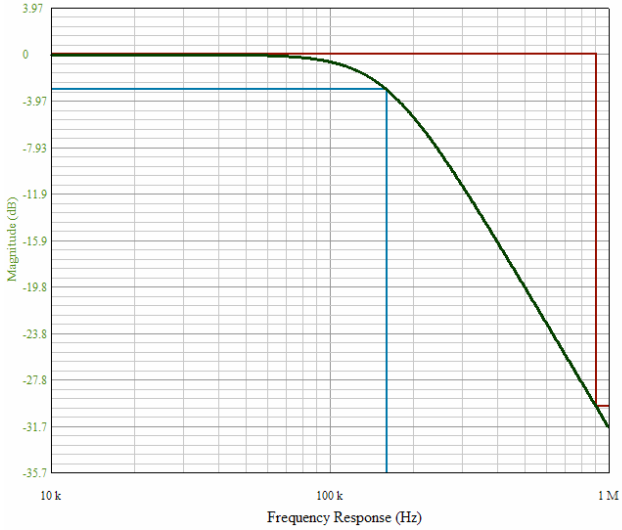
At 320kHz (maximum setting)

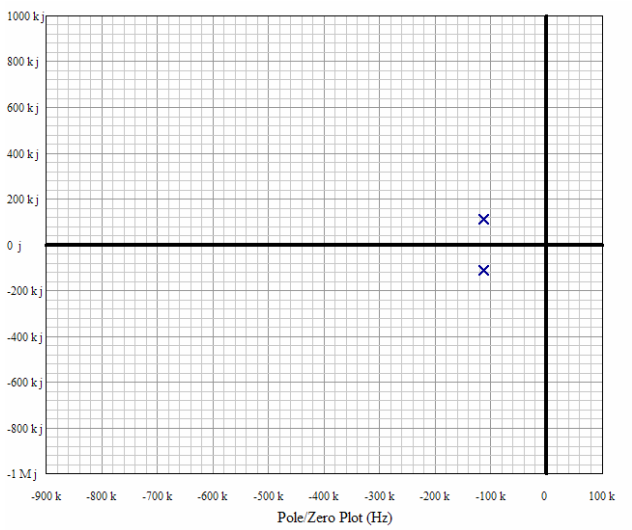
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	320 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	56.5 kHz
Actual Corner Frequency	319.6 kHz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (1.42004e+006-1.42004e+006j))·(S + (1.42004e+006+1.42004e+006j))]		

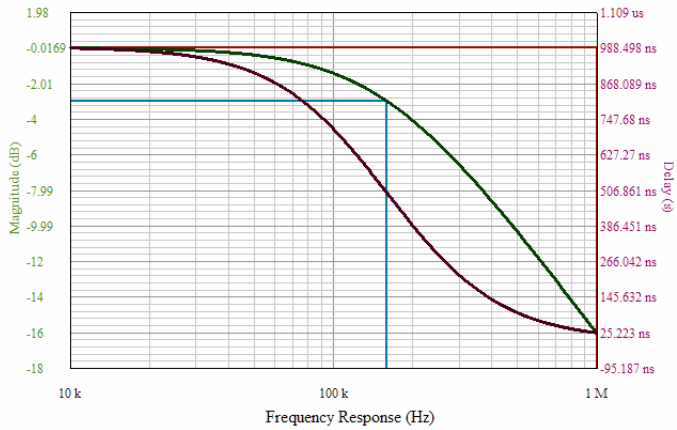
At 1kHz (mimimum setting)

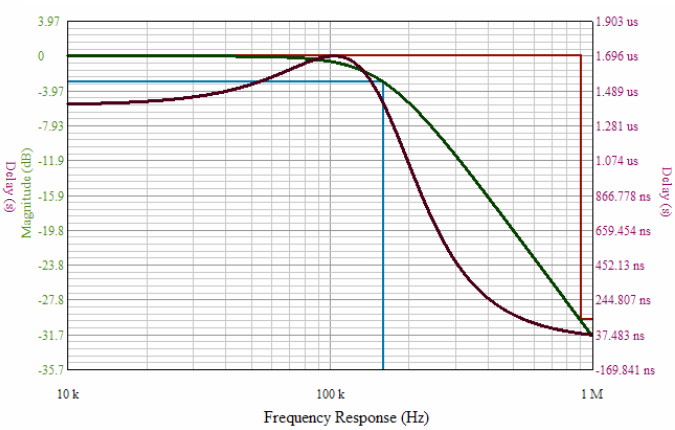
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	1 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	177 Hz
Actual Corner Frequency	998.8 Hz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (4437.61-4437.61j))·(S + (4437.61+4437.61j))]		

Low pass filter, chipset default setting 160 kHz.









At 160kHz (default setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	160 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	905 kHz
Actual Corner Frequency	160.2 kHz		
Filter Transfer Function (Pole/Zero Form)	1.01305e+012 / [(S + (711706-711706j))·(S + (711706+711706j))]		

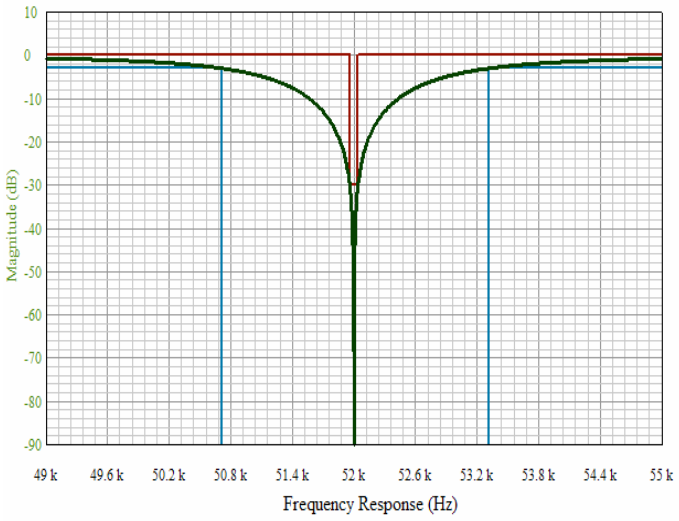
At 640 kHz

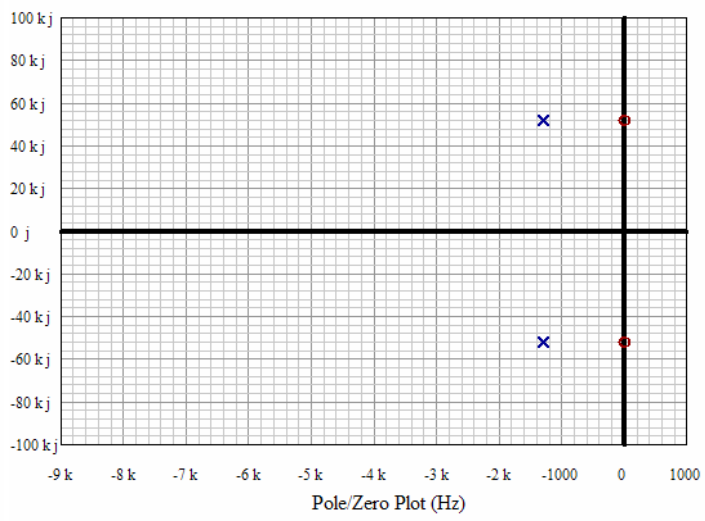
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	640 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	3.62 MHz
Actual Corner Frequency	640.8 kHz		
Filter Transfer Function (Pole/Zero Form)	1.62088e+013 / [((S + (2.84682e+006-2.84682e+006j))·(S + (2.84682e+006+2.84682e+006j)))]		

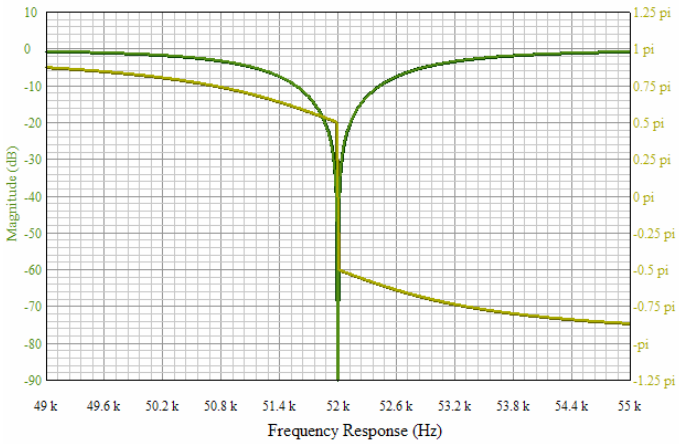
At 2 kHz

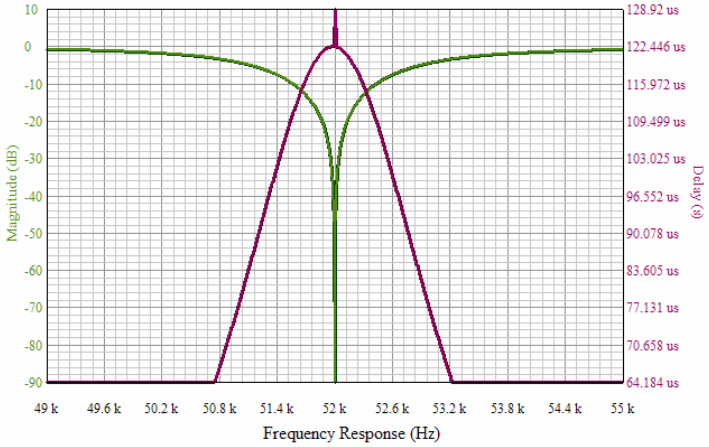
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	2.00 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	11.3 kHz
Actual Corner Frequency	2.00 kHz		
Filter Transfer Function (Pole/Zero Form)	1.58289e+008 / [(S + (8896.32-8896.32j))·(S + (8896.32+8896.32j))]		

Notch filter, Fc = 52 kHz









At 52 kHz (default setting)

Filter Parameters			
Passband Gain	0 dB	Center Frequency	52 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	52 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 326726j)·(S + 326726j) / [(S + (8180.11-326623j))·(S + (8180.11+326623j))]		

At 54 kHz

Filter Parameters			
Passband Gain	0 dB	Center Frequency	54 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	54 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 339292j)·(S + 339292j) / [(S + (8180.11-339193j))·(S + (8180.11+339193j))]		

At 50 kHz

Filter Parameters			
Passband Gain	0 dB	Center Frequency	50 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	50 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 314159j)·(S + 314159j) / [(S + (8180.11-314053j))·(S + (8180.11+314053j))]		

1.2 EPC Gen2 baseband processing circuit (RFID_twin)

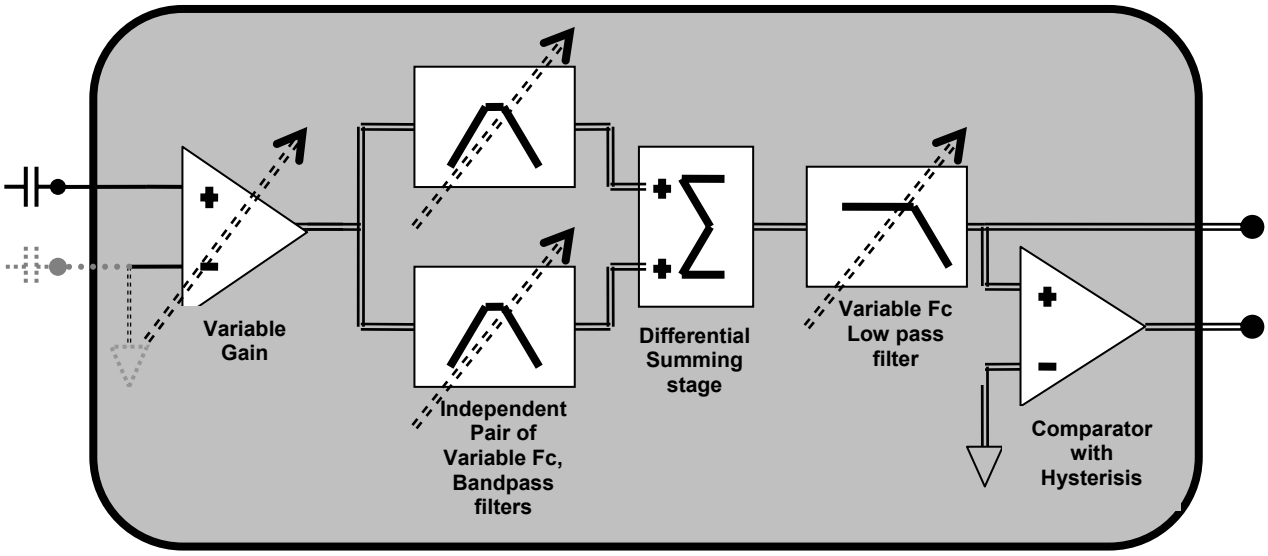


Fig 2: EPC Gen 2 analog baseband processing circuit

The EPC Gen 2 circuit enables the extraction of all data frequency pairs i.e. 2KHz & 4KHz, 32KHz & 64KHz, 320KHz & 640KHz.

Gain stage	Control word G1 to G4	Gain (dB)	Gain	Tolerance	Comment
First gain stage	0000	N/A	N/A	N/A	Only used for Standby.
	0001	0	1.00	0.10%	Inverting differential gain stage,
	0010	6	2.00	0.18%	
	0011	12	3.98	0.50%	
	0100	18	7.94	1.45%	
	0101	24	15.85	1.89%	
	0110	30	31.62	3.03%	
	0111	N/A	N/A	N/A	Not used

	Control word G1 to G4	Additional Gain (dB)	Gain of lower frequency bandpass signal path	Gain of higher frequency bandpass signal path	Additional tolerance	Comment
Summing stage input branch gain.	1000	+3dB	1.4	0	0.10%	If used the first stage gain = 0dB
	1001	+6dB	2.0	0	0.18%	
	1010	+12dB	4.0	0	0.50%	
	1011	Not used	Not used	Not used	Not used	Not used
	1100	+3dB	0	1.4	0.10%	If used the first stage gain = 0dB
	1101	+6dB	0	2.0	0.18%	
	1110	+12dB	0	4.0	0.50%	
	1111	Not used	Not used	Not used	Not used	Not used

If the Summing stage input branch Gain settings are used for the balance, the first gain stage is 0dB.

Lower frequency bandpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
Control word bits LF1 to LF4	2, 4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 424		Better than 1%	2nd Order Biquadratic, Butterworth approximation Bandpass Gain=1 Quality factor = 0.707 Inverting architecture
Higher frequency bandpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
Control word bits HF1 to HF4	4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 640, 848.		Better than 1%	2nd Order Biquadratic, Butterworth approximation Bandpass Gain=1 Quality factor = 0.707 Inverting architecture
Lowpass filter	Fc (-6dB corner frequency)		Tolerance	Comment
Band limiting filter,	Corner frequency is always 1.5 x "higher frequency bandpass filter" corner frequency	6kHz to 1270kHz	Better than 2%	1st order Bilinear. Fc is -6dB amplitude w.r.t zero dB passband.
Comparator		Hysterisis	Tolerance	Comment
		570mV	10%	Complimentary outputs available
See graphical data for filter response details (Next pages).				

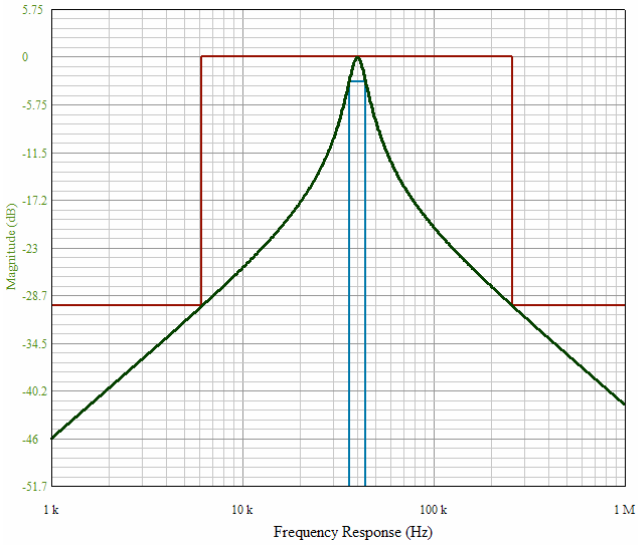
The Control word as it applies to Circuit 2, RFID_twin

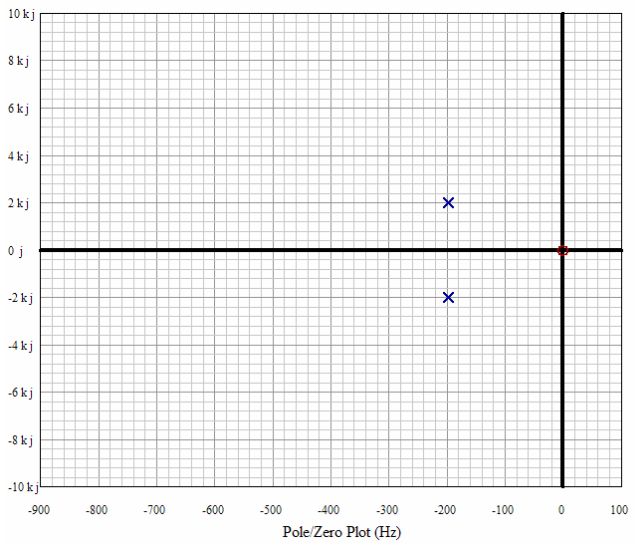
ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)															
Select circuit		**Notch filter center frequency**		**Gain control**				**Lower subcarrier frequency (this sets lower bandpass or Highpass filter)**				**Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)**			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														**LSB**
A1	**A2**	**A3**	**A4**	**G1**	**G2**	**G3**	**G4**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
01 = EPCGen2 (TWIN) filter		Not used		G1,G2,G3,G4	Bulk Gain	LF gain (Note6)	HF gain (Note7)	LF1,LF2, LF3,LF4		Freq (KHz)		HF1,HF2, HF3.HF4		Freq (KHz)	
				0000	*Note5*	*Note5*	*Note5*	0000		2		0000		4	
				0001	**0dB**	+0dB	+0dB	0001		4		0001		8	
				0010	+6dB	+0dB	+0dB	0010		8		0010		16	
				0011	+12dB	+0dB	+0dB	0011		16		0011		20	
				0100	+18dB	+0dB	+0dB	0100		20		0100		32	
				0101	+24dB	+0dB	+0dB	0101		32		0101		40	
				0110	+30dB	+0dB	+0dB	**0110**		**40**		0110		64	
				0111		Not used		0111		64		0111		80	
				1000	+0dB	+3dB	+0dB	1000		80		1000		106	
				1001	+0dB	+6dB	+0dB	1001		106		1001		128	
				1010	+0dB	+12dB	+0dB	1010		128		1010		160	
				1011		Not used		1011		160		1011		212	
				1100	+0dB	+0dB	+3dB	1100		212		1100		256	
				1101	+0dB	+0dB	+6dB	1101		256		**1101**		**320**	
				1110	+0dB	+0dB	+12dB	1110		320		1110		640	
				1111		Not used		1111		424		1111		848	

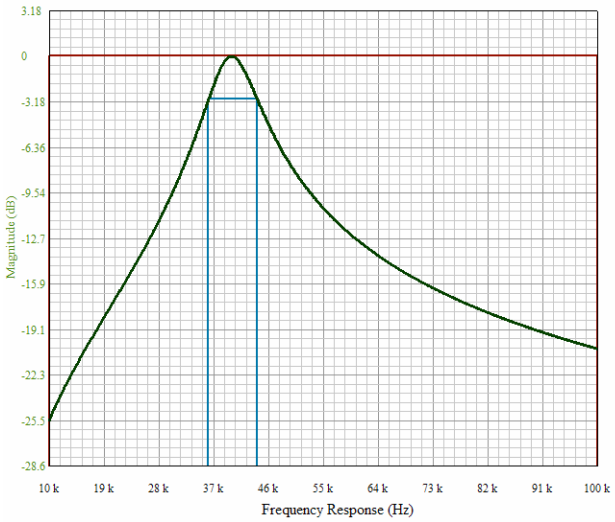
Notes
5) Control word 0000000000000000(binary), 0x00, 0x00 (Hex) sets the chipset into standby (low power mode)
6) Nominal gain = 0dB. higher gain for Lower bandpass v.s. higher bandpass
7) Nominal gain = 0dB. higher gain for higher bandpass v.s. lower bandpass

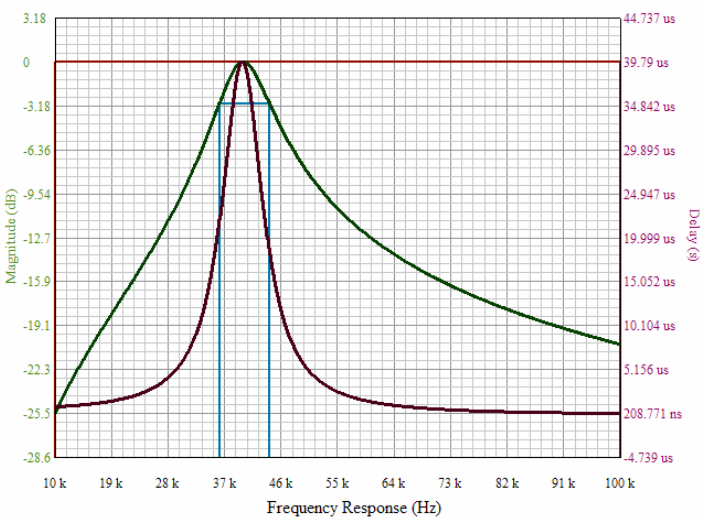
Bandpass filter characteristics, these apply to either the “high” or “low” bandpass filter, each has the same filter architecture and performance.

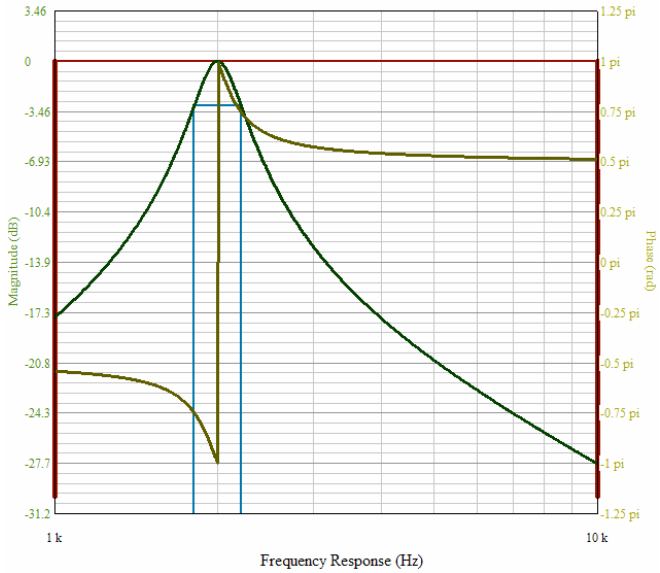
40kHz, Bandpass filter.









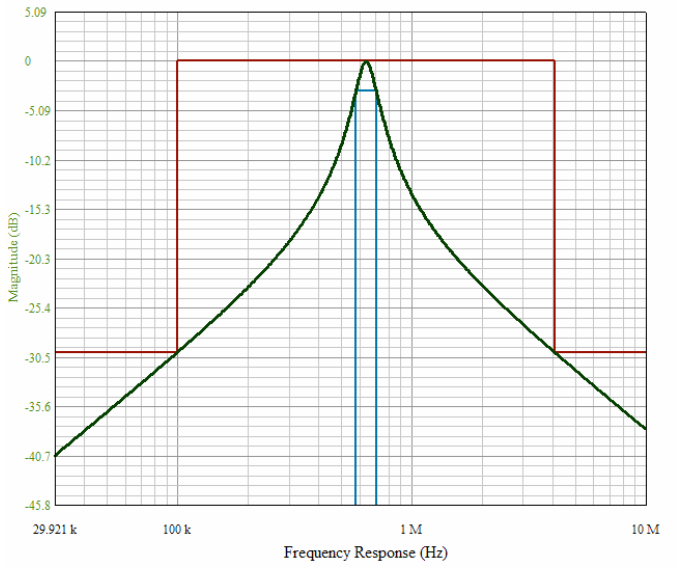


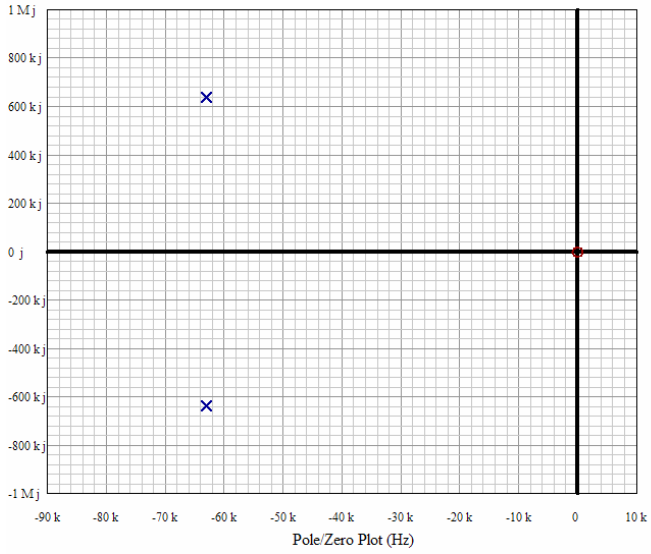
Filter Parameters	
Passband Gain	0 dB
Center Frequency	40 kHz
Stop Band Attenuation	30 dB
Pass Band Width	8 kHz
Stop Band Width	254 kHz
Quality Factor	4.99

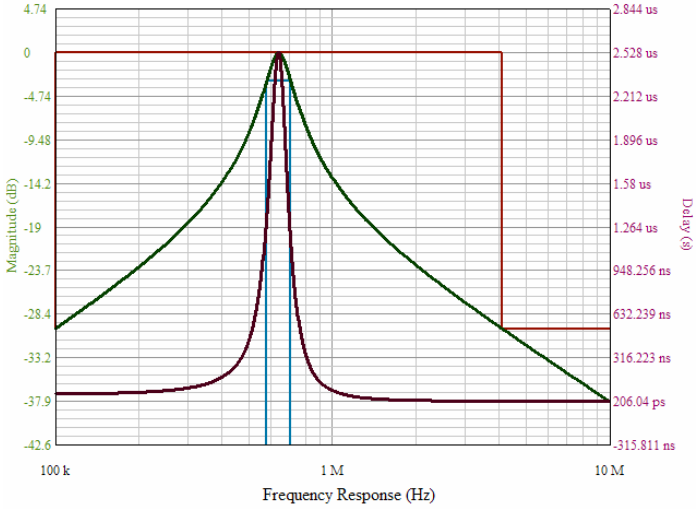
Filter Transfer Function - (Pole/Zero Form)

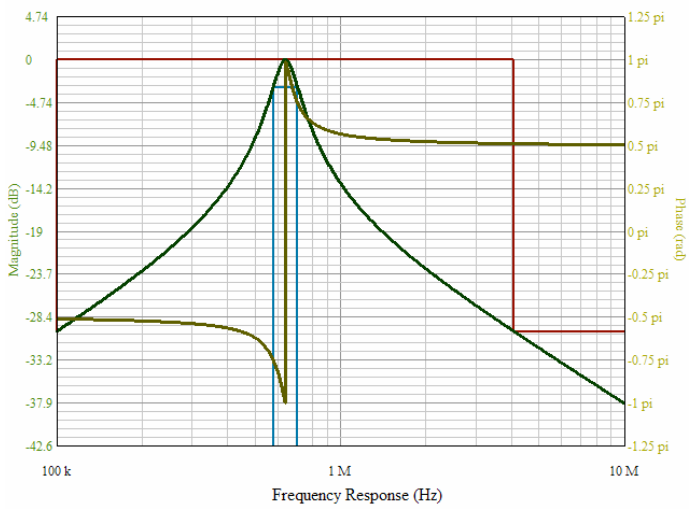
$$\frac{50385 \cdot (S)}{[(S + (25192.5-250062j))\cdot(S + (25192.5+250062j))]}$$

640kHz, Bandpass filter.







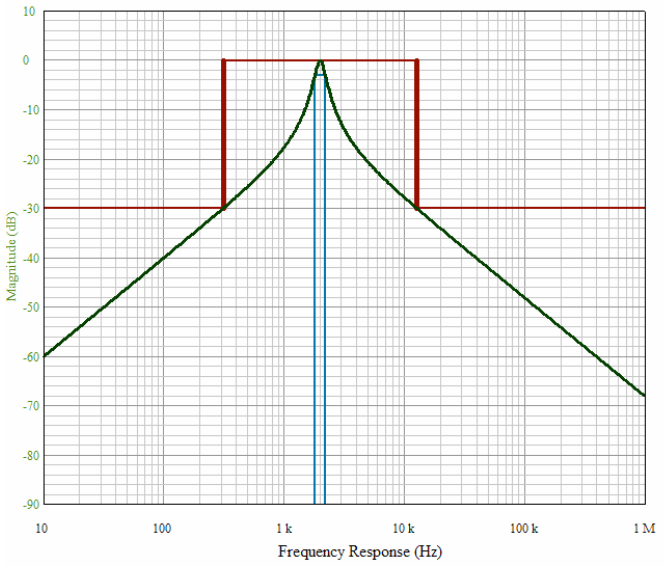


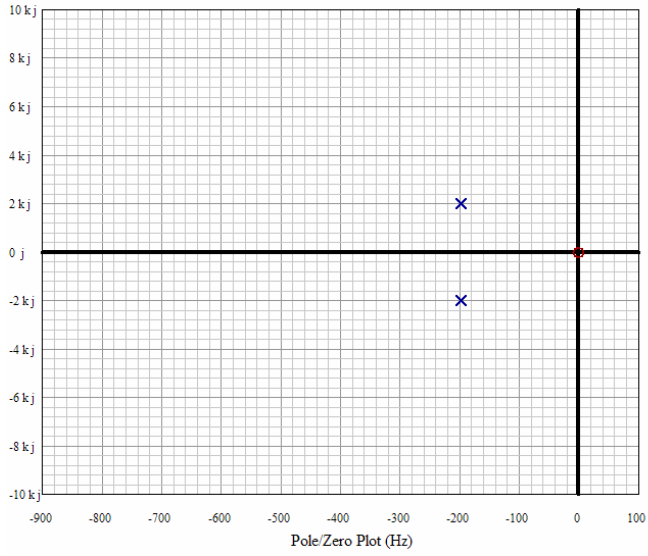
Filter Parameters	
Passband Gain	0 dB
Center Frequency	640 kHz
Stop Band Attenuation	30 dB
Pass Band Width	128 kHz
Stop Band Width	4 MHz
Quality Factor	5.07

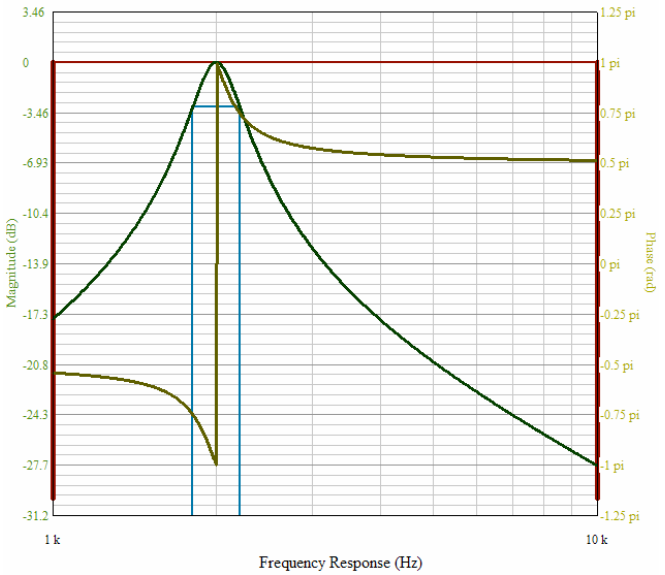
Filter Transfer Function - (Pole/Zero Form)

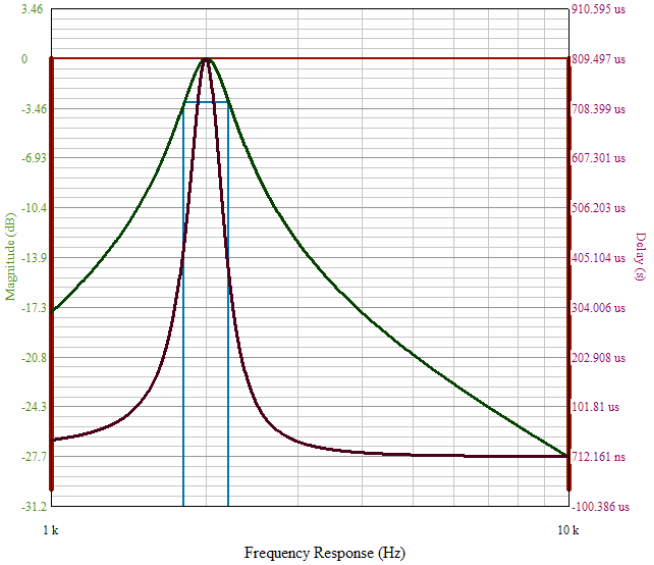
$$\frac{792442 \cdot (S)}{[(S + (396221-4.00167e+006j))\cdot(S + (396221+4.00167e+006j))]}$$

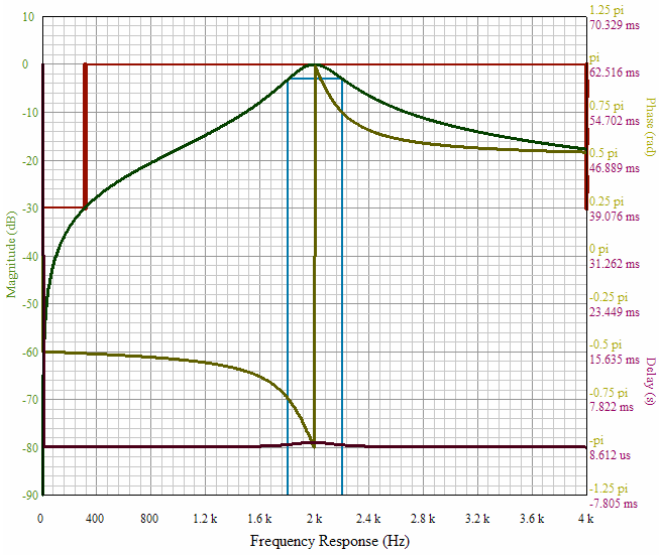
2kHz, Bandpass filter











Filter Parameters	
Passband Gain	0 dB
Center Frequency	2 kHz
Stop Band Attenuation	30 dB
Pass Band Width	400 Hz
Stop Band Width	12.5 kHz
Quality Factor	5.07

Filter Transfer Function - (Pole/Zero Form)

$$\frac{2476.38 \cdot (S)}{[(S + (1238.19-12505.2j))\cdot(S + (1238.19+12505.2j))]}$$

1.3 EPC Gen2 baseband processing circuit (RFID_triple)

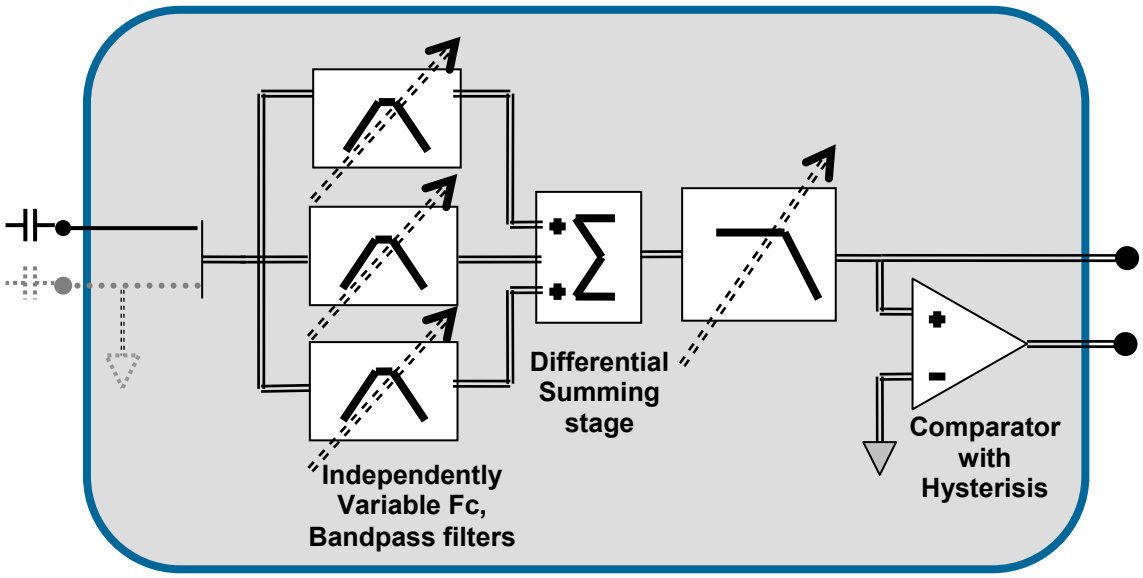


Fig 3: EPC Gen 2 Analog baseband processing circuit.

The EPC gen 2 Triple circuit enables extraction of three parallel sub-carrier signals without circuit modification - e.g. Synchronization frequency and data frequency pair - 42KHz & 64KHz, 128KHz (Many other frequency combinations possible).
This circuit does not include the anti-saturation switch and control pin.
This circuit does not include the first gain stage, This circuit implements the gain and balance control within the summing stage.

Gain stage	Control word G1 to G4	Gain (dB)	Gain (A1		Tolerance (A2)	Comment
First gain stage	0000	N/A	N/A		N/A	Only used for Standby.
	0001	0	1.00		0.10%	Realized in the summing stage
	0010	6	2.00		0.18%	
	0011	12	3.98		0.50%	
	0100	18	7.94		1.45%	
	0101	24	15.85		1.89%	
	0110	30	31.62		3.03%	
	0111	N/A	N/A		N/A	Not used
	Control word G1 to G4	Additional Gain (dB)	Gain of lower frequency bandpass signal path	Gain of higher frequency bandpass signal path	Additional tolerance	Comment
Summing stage input branch gain. *(If these are used the first stage gain = 0dB)*	1000	+3dB	1.4	0	0.10%	If used the first stage gain = 0dB The balance gain of the 1/3 frequency band is adjusted with and to the same value as the highest frequency bandpass.
	1001	+6dB	2.0	0	0.18%	
	1010	+12dB	4.0	0	0.50%	
	1011	Not used	Not used	Not used	Not used	Not used
	1100	+3dB	0	1.4	0.10%	If used the first stage gain = 0dB
	1101	+6dB	0	2.0	0.18%	
	1110	+12dB	0	4.0	0.50%	
	1111	Not used	Not used	Not used	Not used	Not used

Lower frequency bandpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
Control word bits LF1 to LF4	2, 4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 424		Better than 1%	2nd Order Biquadratic, Butterworth approximation Bandpass Gain=1 Quality factor = 0.707 Inverting architecture
Higher frequency bandpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
Control word bits HF1 to HF4	4, 8, 16, 20, 32, 40, 64, 80, 106, 128, 160, 212, 256, 320, 640, 848.		Better than 1%	2nd Order Biquadratic, Butterworth approximation Bandpass Gain=1 Quality factor = 0.707 Inverting architecture
Third frequency bandpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
The center frequency of this bandpass is always one third of the frequency of "Higher frequency bandpass filter"	1.3, 2.6, 5.3, 6.6, 10.6, 13.3, 21.3, 26.6 35.3, 42.6, 53.3, 70.6 85.3, 106.6, 213.3, 282.6		Better than 1%	2nd Order Biquadratic, Butterworth approximation Bandpass Gain=1 Quality factor = 0.707 Inverting architecture
Lowpass filter	Fc (-6dB corner frequency)	Tolerance	Comment	
Band limiting filter,	Corner frequency is always 1.5 x "higher frequency bandpass filter" corner frequency	6kHz to 1270kHz	Better than 2%	1st order Bilinear. Fc is -6dB amplitude w.r.t zero dB passband.
Comparator		Hysterisis	Tolerance	Comment
		570mV	10%	Complimentary outputs available
See graphical data for filter response details (Next pages).				

The Control word as it applies to Circuit 3, RFID_triple

ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)

Select circuit		Notch filter center frequency		Gain control				Lower subcarrier frequency (this sets lower bandpass or Highpass filter)				Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														LSB
A1	A2	A3	A4	G1	G2	G3	G4	LF1	LF2	LF3	LF4	HF1	HF2	HF3	HF4
00 = Tripleband Bandpass		Not used		G1,G2,G3, G4	Bulk Gain	LF gain (Note6)	HF gain (Note7 and 10)	LF1,LF2, LF3,LF4		Freq (KHz)		HF1,HF2, HF3.HF4		Freq (KHz)	
				0000	*Note5*	*Note5*	*Note5*	0000		2		0000		4	
				0001	**0dB**	+0dB	+0dB	0001		4		0001		8	
				0010	+6dB	+0dB	+0dB	0010		8		0010		16	
				0011	+12dB	+0dB	+0dB	0011		16		0011		20	
				0100	+18dB	+0dB	+0dB	0100		20		0100		32	
				0101	+24dB	+0dB	+0dB	0101		32		0101		40	
				0110	+30dB	+0dB	+0dB	**0110**		**40**		0110		64	
				0111		Not used		0111		64		0111		80	
				1000	+0dB	+3dB	+0dB	1000		80		1000		106	
				1001	+0dB	+6dB	+0dB	1001		106		1001		128	
				1010	+0dB	+12dB	+0dB	1010		128		1010		160	
				1011		Not used		1011		160		1011		212	
				1100	+0dB	+0dB	+3dB	1100		212		1100		256	
				1101	+0dB	+0dB	+6dB	1101		256		**1101**		**320**	
				1110	+0dB	+0dB	+12dB	1110		320		1110		640	
				1111		Not used		1111		424		1111		848	

Notes
3) lowest filter corner frequency is always one third of the highest frequency, the summing stage input branch gain=+6db Fixed
6) Nominal gain = 0dB. higher gain for Lower bandpass v.s. higher bandpass
7) Nominal gain = 0dB. higher gain for higher bandpass v.s. lower bandpass
10) The balance gain of the 1/3 frequency bandpass filter is adjusted with and to the same value as the highest frequency bandpass filter.

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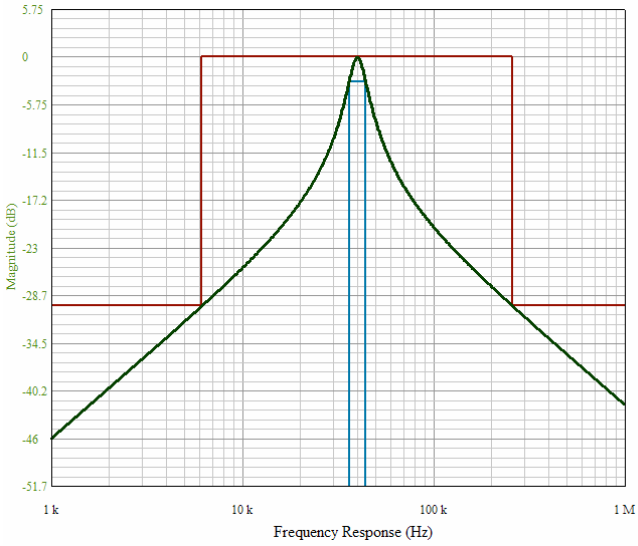
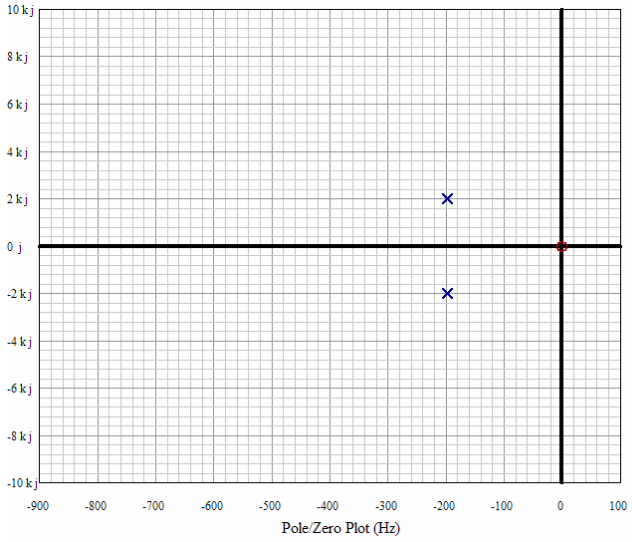
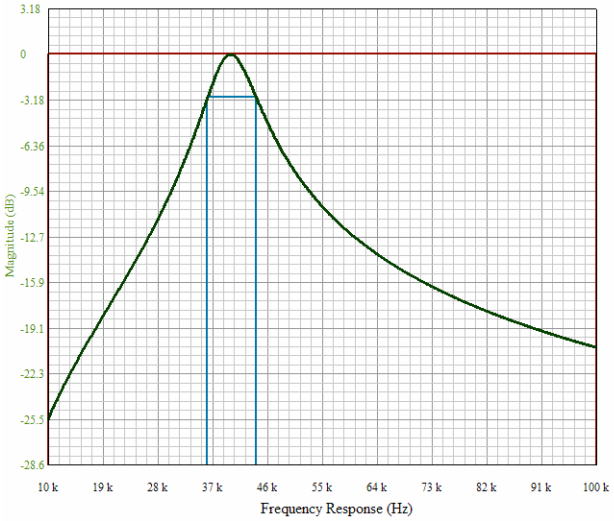
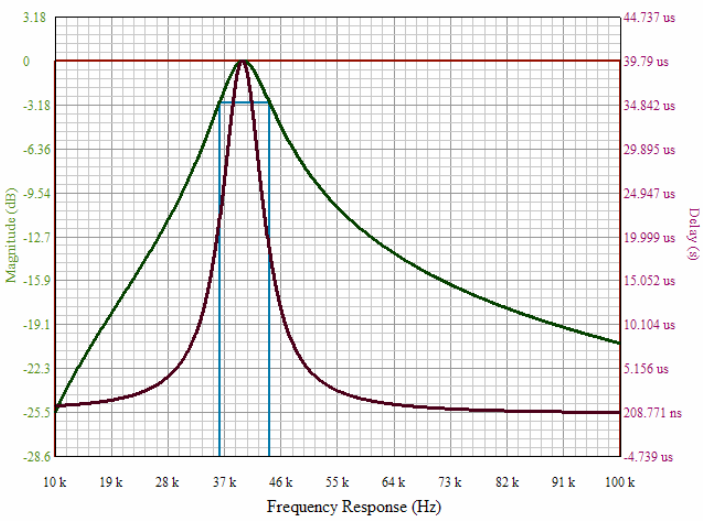
Bandpass filter characteristics, these apply to any of the “bandpass filter”, each has the same filter architecture and performance.

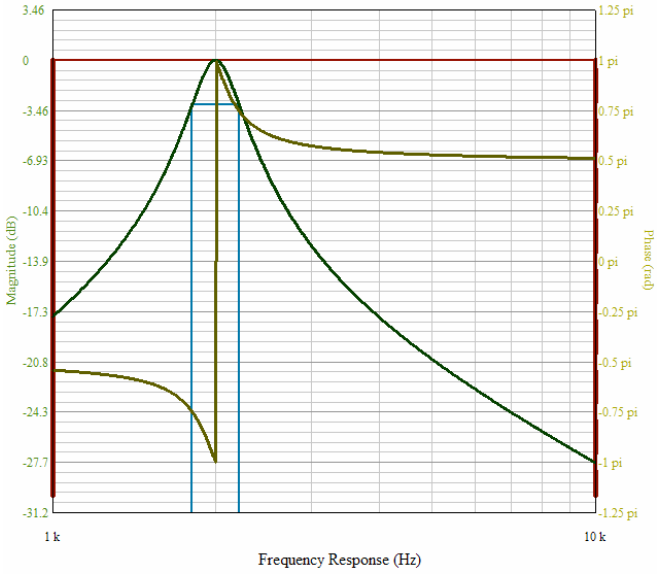
40kHz, Bandpass filter.









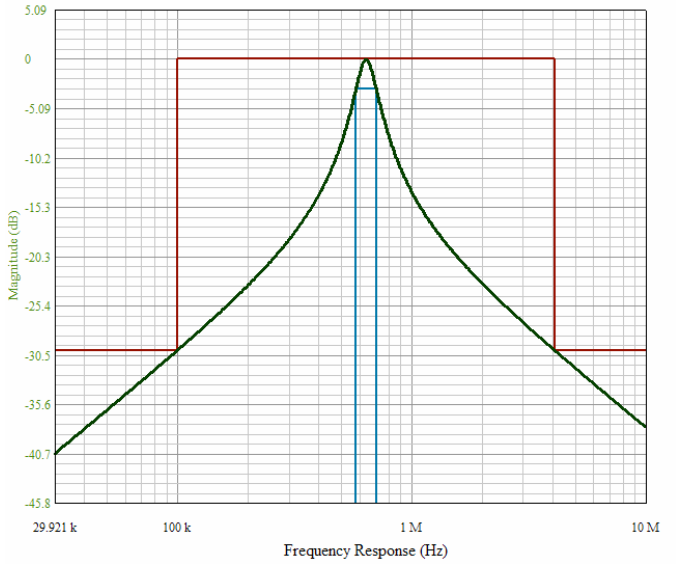


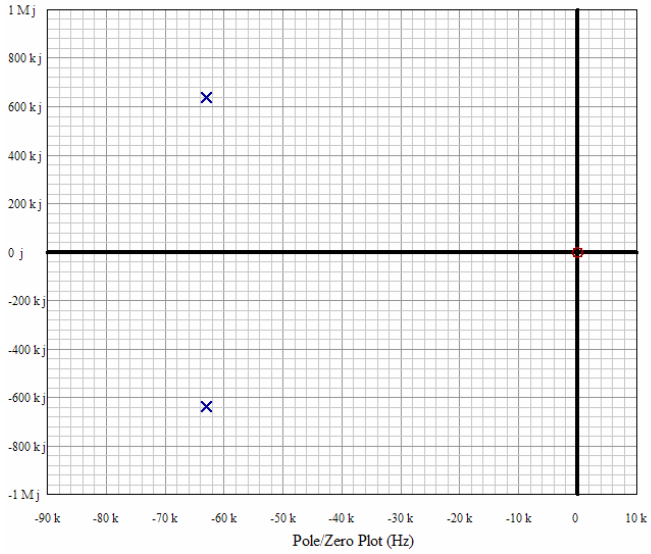
Filter Parameters	
Passband Gain	0 dB
Center Frequency	40 kHz
Stop Band Attenuation	30 dB
Pass Band Width	8 kHz
Stop Band Width	254 kHz
Quality Factor	4.99

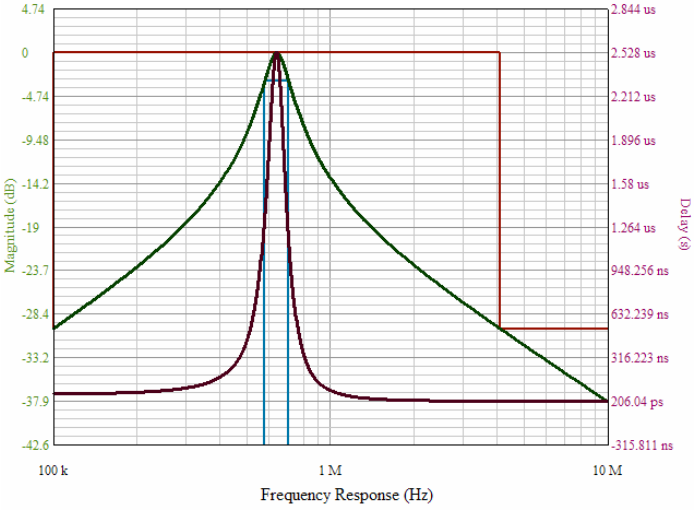
Filter Transfer Function - (Pole/Zero Form)

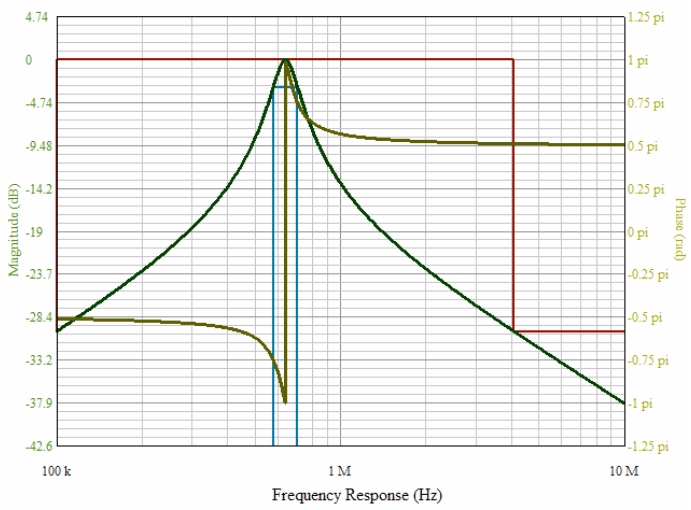
$$\frac{50385 \cdot (S)}{[(S + (25192.5-250062j))\cdot(S + (25192.5+250062j))]}$$

640kHz, Bandpass filter.







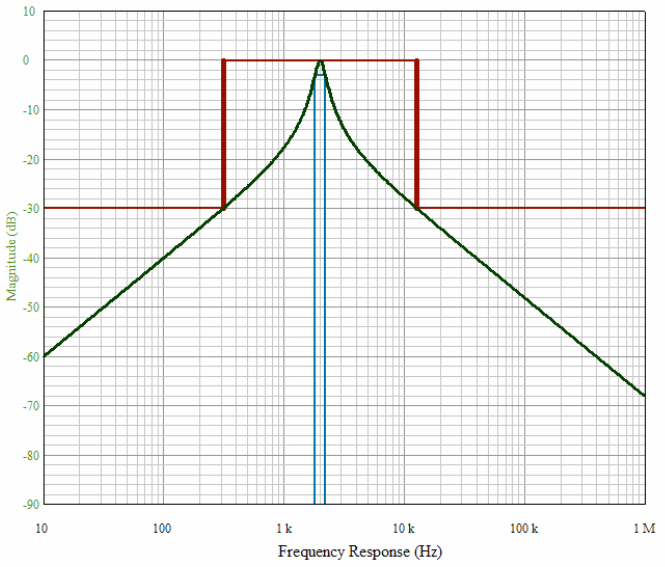


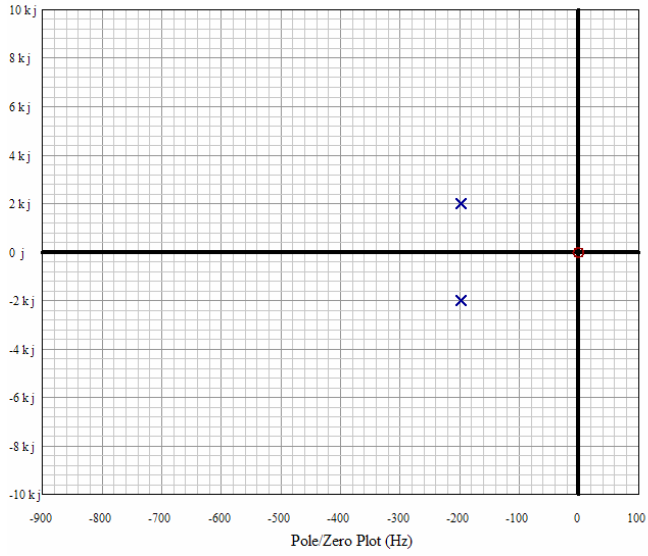
Filter Parameters	
Passband Gain	0 dB
Center Frequency	640 kHz
Stop Band Attenuation	30 dB
Pass Band Width	128 kHz
Stop Band Width	4 MHz
Quality Factor	5.07

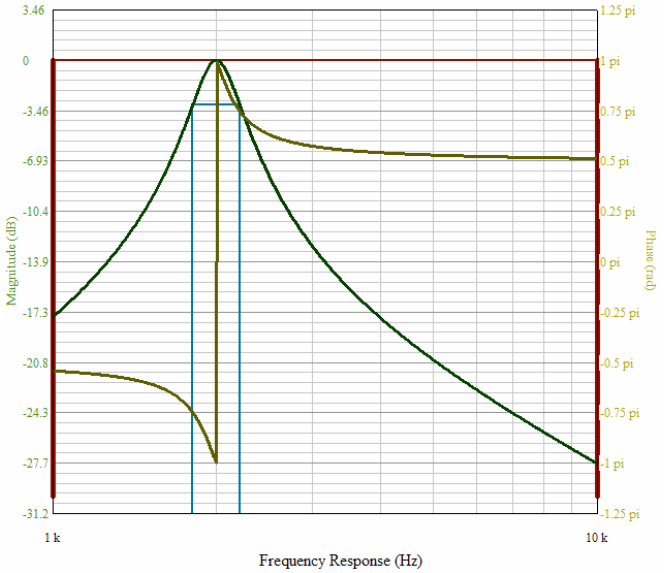
Filter Transfer Function - (Pole/Zero Form)

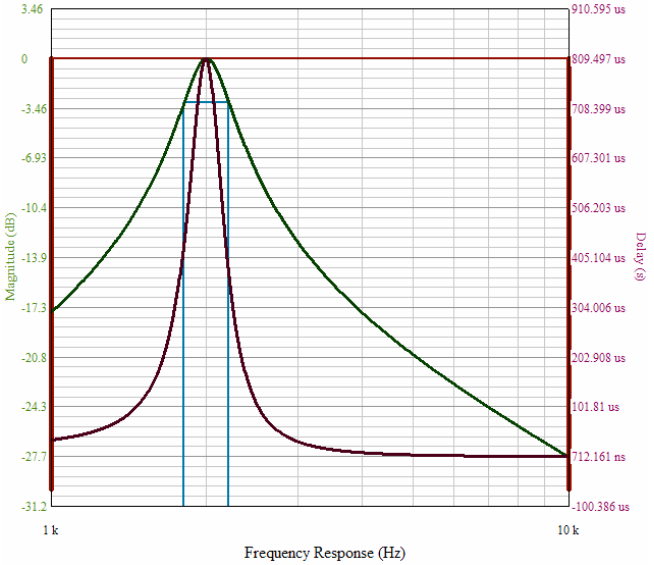
$$\frac{792442 \cdot (S)}{[(S + (396221-4.00167e+006j))\cdot(S + (396221+4.00167e+006j))]}$$

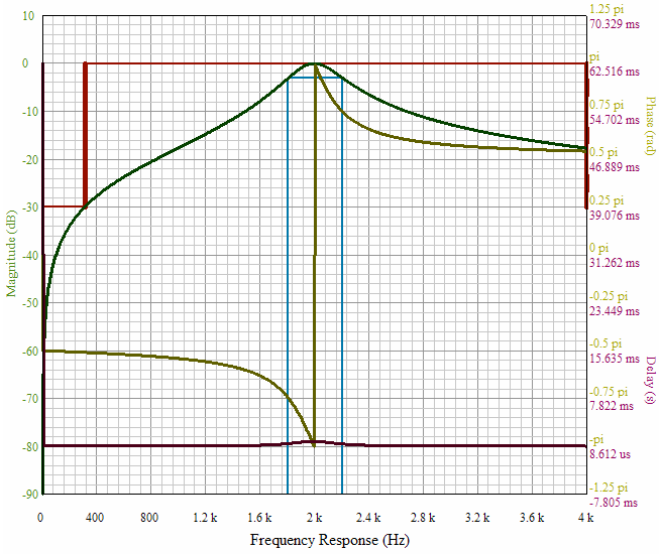
2kHz, Bandpass filter











Filter Parameters	
Passband Gain	0 dB
Center Frequency	2 kHz
Stop Band Attenuation	30 dB
Pass Band Width	400 Hz
Stop Band Width	12.5 kHz
Quality Factor	5.07

Filter Transfer Function - (Pole/Zero Form)

$$\frac{2476.38 \cdot (S)}{[(S + (1238.19-12505.2j))\cdot(S + (1238.19+12505.2j))]}$$

1.4 2.2MHz and 3.3MHz signal processing circuit (RFID_fast)

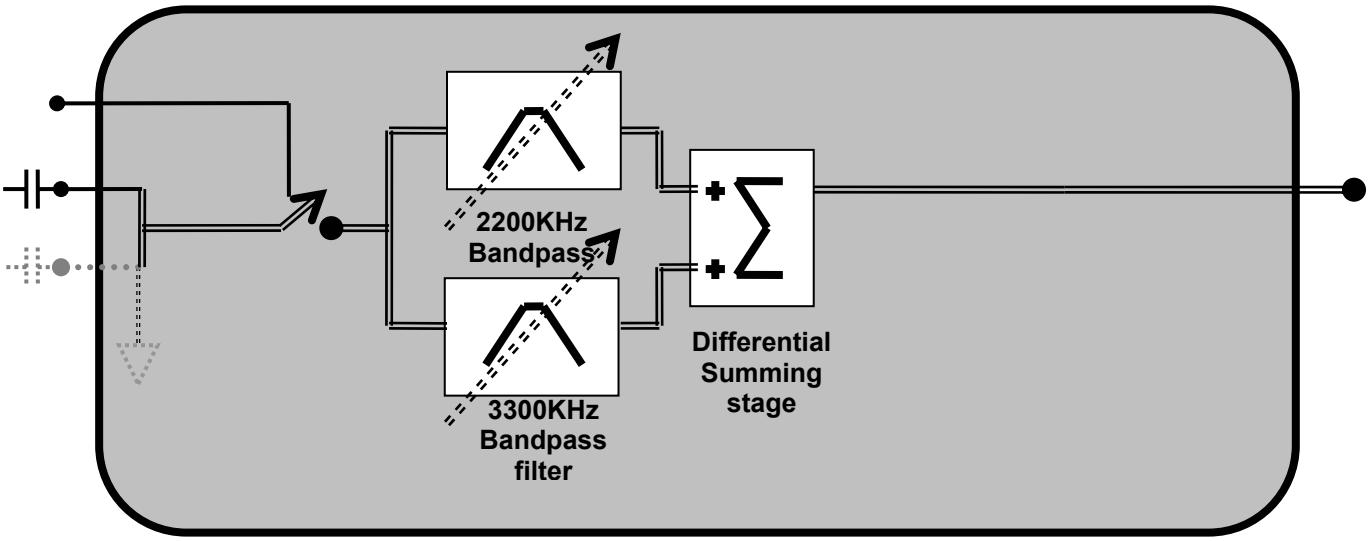


Fig 4 EPC Gen 2 analog baseband processing circuit

This circuit is specifically designed to filter and extract data from input sub-carrier signals at 2.2MHz/3.3MHz., there are no variables

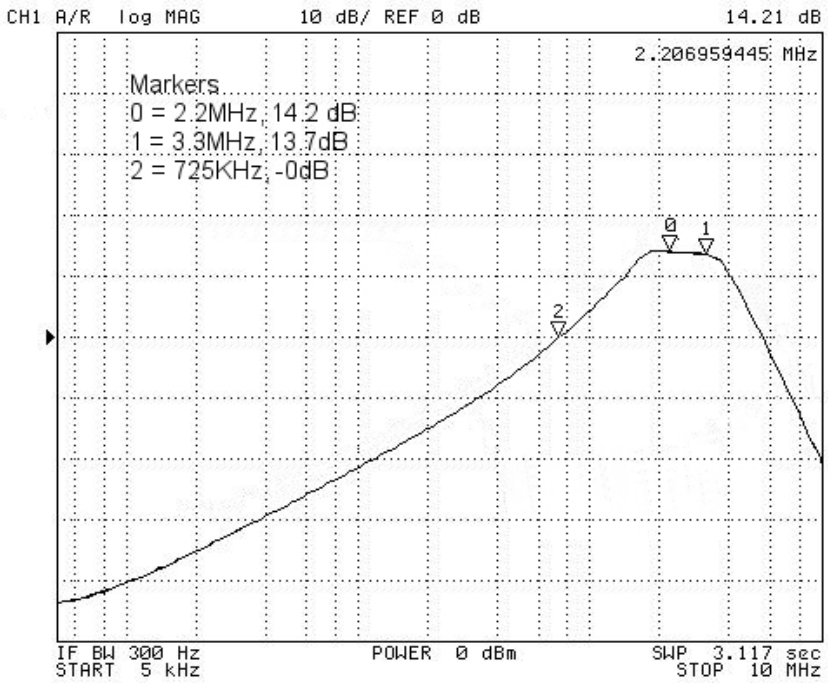
Lower bandpass filter	Fc (Center Frequency. kHz)	Gain (dB)	Gain	Tolerance	Comment
	3300	6.0	2.0	Better than 5%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1, Qf = 30
Higher bandpass filter	Fc (Center Frequency, kHz)	Gain (dB)	Gain	Tolerance	Comment
	2200	6.0	2.0	Better than 5%	3nd Order custom filter Gain=1, Q = 5
Summing stage		Gain (dB)	Gain	Gain (dB)	Comment
	Upper input branch (2200KHz)	18	8	Better than 5%	
	Lower input branch (3300KHz)	18	8	Better than 5%	
Signal path	Description	Gain (dB)	Gain	Tolerance	Comment
	3300KHz sin\gnal frequencies	24	16	5%	
	2200KHz signal frequencies	24	16	5%	
See graphical date for filter response details (Next pages).					

The Control word as it applies to Circuit 1, RFID_fast.

ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)															
Select circuit		**Notch filter center frequency**		**Gain control**				**Lower subcarrier frequency (this sets lower bandpass or Highpass filter)**				**Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)**			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														**LSB**
A1	**A2**	**A3**	**A4**	**G1**	**G2**	**G3**	**G4**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
10 = "Class0" bandpass		B1,B2	Freq (kHz)	G1,G2,G3,G4				LF1,LF2, LF3,LF4				HF1,HF2,HF3.HF4			
		Not used		Not used				Not used				Not used			

Notes
2 “Class0", 2.2/3.3MHz Gain = 0dB. No bulk gain or balance control

RFID_fast Overall Signal path filter Characteristics,



1.5 Anti-saturation, RFID dpASP input control.

Anti-saturation feature of this chipset allows the user to isolate the RFID dpASP filter input stage from the input signal, whilst maintaining all circuit bias points. This provides the user with a mechanism which can be used to mask out the high energy transmit signal from the low energy receive signal within an RFID card reader unit; avoiding potential receiver saturation.

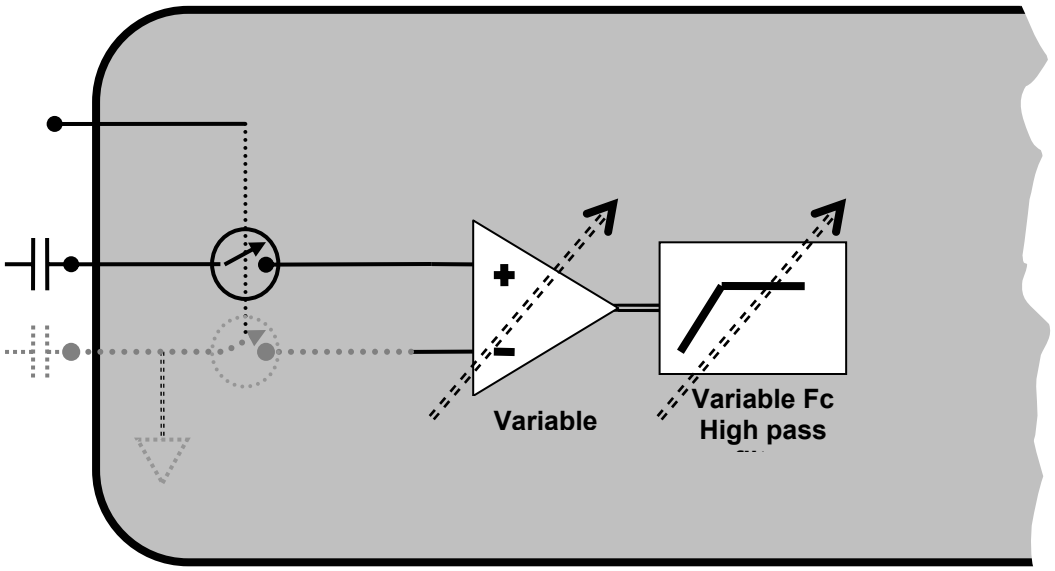


Fig 5, Anti-saturation feature

Timing control.

The state of the Input isolation switch is set by a 3.3v logic signal applied to the ON/OFFb pin.
This Pin is 19, named IO7P.
A logic high (3.3 volts), will open the switches.
A logic low (0.0 volts) will close the switches.
i.e. Anti-saturation active, IO7P = high, switches are open

On the AN238K04 Evaluation board this signal is named "EXECUTE".

1.6 The control word

The exact circuit configuration which is active within the RFID dpASP is defined by the content of the 16 bit control word, within the AN238C04 State Machine.

This table define the entire control word

ANADIGM RangeMaster2 Control Interface (16 Bit Control Byte)

Select circuit		Notch filter center frequency		Gain control				Lower subcarrier frequency (this sets lower bandpass or Highpass filter)				Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)			
MSB	LOAD MSB first. LSB last as two separate words into the Rangemaster RFID State Machine														LSB
A1	**A2**	**A3**	**A4**	**G1**	**G2**	**G3**	**G4**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
A1A2, 00 = Universal (WIDE) bandpass A1A2, 01 = EPCGen2 (TWIN) filter A1A2, 10 = "Class0" bandpass *(see Note2)* A1A2, 11 = Tripleband filter *(Note 3)*		B1,B2	Freq (kHz)	G1,G2,G3,G4	Bulk Gain	LF gain (Note6)	HF gain (Note7 and 10)	LF1,LF2, LF3,LF4		Freq (KHz)		HF1,HF2, HF3.HF4		Freq (KHz)	
		00	*Note4*	0000	*Note5*	*Note5*	*Note5*	0000		2		0000		4	
		01	**50.0**	**0001**	**0dB**	+0dB	+0dB	0001		4		0001		8	
		10	52.0	0010	+6dB	+0dB	+0dB	0010		8		0010		16	
		11	54.0	0011	+12dB	+0dB	+0dB	0011		16		0011		20	
				0100	+18dB	+0dB	+0dB	0100		20		0100		32	
				0101	+24dB	+0dB	+0dB	0101		32		0101		40	
				0110	+30dB	+0dB	+0dB	**0110**		**40**		0110		64	
				0111		Not used		0111		64		0111		80	
				1000	+0dB	+3dB	+0dB	1000		80		1000		106	
				1001	+0dB	+6dB	+0dB	1001		106		1001		128	
				1010	+0dB	+12dB	+0dB	1010		128		1010		160	
				1011		Not used		1011		160		1011		212	
				1100	+0dB	+0dB	+3dB	1100		212		1100		256	
				1101	+0dB	+0dB	+6dB	1101		256		**1101**		**320**	
				1110	+0dB	+0dB	+12dB	1110		320		1110		640	
				1111		Not used		1111		424		1111		848	

Notes

1) bold - Bold text indicates the default circuit, the RangeMaster chipset will start-up with this circuit
the chipset starts up with this circuit after power up or reset,
but, if the chipset is awakened from sleep (by a dummy config) then it remembers the circuit it had before it went to sleep.

2)"Class0", 2.2/3.3MHz Gain = 0dB. No bulk gain or balance control –

3) lowest filter corner frequency is always one third of the highest frequency, the summing stage input branch gain=+6db Fixed

4) The notch filter is removed from the signal path. Notch filter is only used in the Universal WIDE filter

5) Control word 0000000000000000(binary), 0x00, 0x00 (Hex) sets the chipset into standby (low power mode)

6) Nominal gain = 0dB. higher gain for Lower bandpass v.s. higher bandpass

7) Nominal gain = 0dB. higher gain for higher bandpass v.s. lower bandpass

8) The anti-saturation control is via a hardware pin only

9) The "Auto-nulling" of all FPAA OpAmps shall be performed at each full reset/power-up cycle.

10) The balance gain of the 1/3 frequency band is adjusted with and to the same value as the highest frequency bandpass.

Examples

00 00 0000 0000 0000	Note 5, Special case, circuit in standby mode.			
00 01 0010 1000 1010	Wide circuit, 50 KHz Notch filter	Circuit Gain = +6dB	Lower subcarrier filter center frequency 80KHz	Higher subcarrier filter center frequency 160KHz

1.7 INTERFACE BETWEEN SYSTEM CONTROLLER AND RFID STATE MACHINE

RangeMaster2 16-bit Control Word - Input Specification

Introduction
This Section describes the interface used by RangeMaster2 to input the 16-bit control word.

Functional Description
The interface for entering the 16-bit control word to the RangeMaster2 chipset is a 3-pin SPI type interface. The control word is entered as 2 bytes, the most significant byte first, each byte with the most significant bit first. An active low select signal is used to tell the interface to expect each byte. The interface must be deselected between the 2 bytes for a minimum period given in the timings below. The interface expects to receive 2 bytes and will wait (hang) until it sees the second byte. The user must ensure that 2 bytes are entered every time the control word is to be changed.

Hardware
This table shows the pins used by this interface.

Pin name	Pin type	Description
SSb	Input	Slave select
SCK	Input	Serial clock
SDI	Input	Serial data in

Timings
This table and figure 6 show the timings specifications.

Symbol	Description	Min	units
T1	SSb falling to SCK rising	500	ns
T2	SSb rising after SCK falling	790	ns
T3	SSb high period Note11	6.5	us
T4	SDI setup to SCK rising	100	ns
T5	SDI hold after SCK rising	100	ns
T6	SCK low period	520	ns
T7	SCK high period	520	ns

Note 11. This is the minimum high period for SSb between the 2 bytes of the control word. There is no maximum time for this. The interface will wait indefinitely for the second byte before the software can continue.

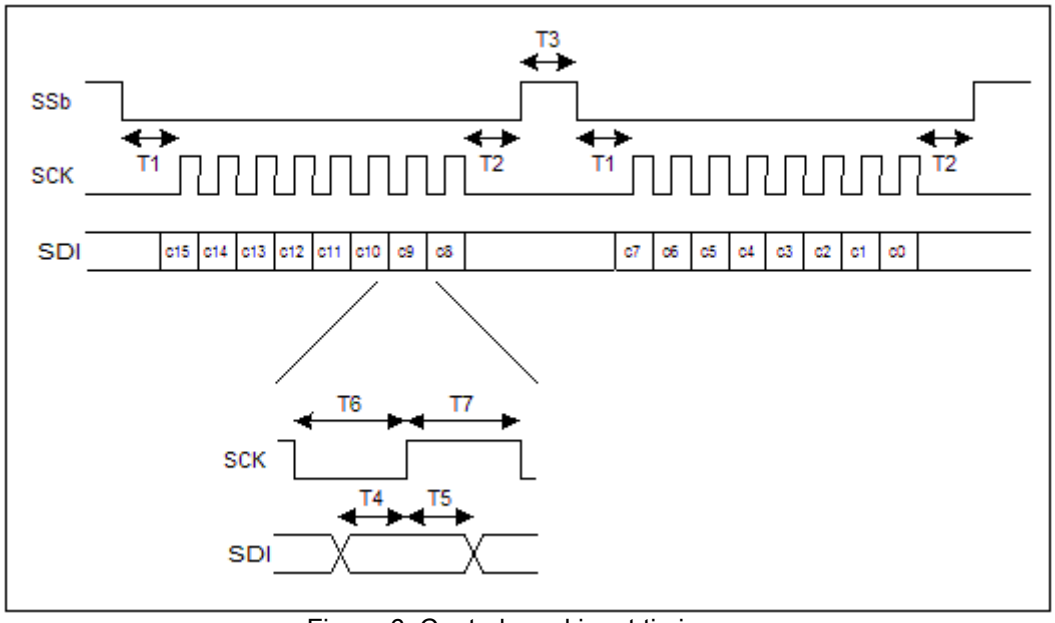


Figure 6: Control word input timings

Special functions - additional timing information

Initial power-up

The RangeMaster2 chipset will immediately start to configure itself, after this is complete the chipset puts itself into Sleep/standby mode, However it has load the default circuit.
The default circuit is
Control word 00 01 0001 0110 1101
Universal wide circuit, 50KHz notch filter, first stage gain = 0dB, Highpass filter corner = 40KHz, Lowpass filter corner =320KHz
See: Note1 of the Control byte table.

Standby and Wake-up

Standby
To put the chipset (AN238E04 and AN238C04) into standby mode, send the control word "00xh, 00xh" to the chipset state machine. Standby mode invokes the following actions;-
The RFID State Machine stops the external oscillator module by de-asserting OSCen
Then the RFID State Machine puts itself into sleep mode.
When the watchdog timer within the AN238E04 dpASP is not reset by the ACLK, the dpASP to go into standby.

The watchdog timeout (period of no clock before sleep mode is started) = minimum 32usec, maximum 100usec.
Sleep mode removes all bias current internally to the dpASP stopping all analog resource current consumption, configuration data is not affected.
Circuit restart is immediately after the first rising clock edge on the ACLK pin, (1usec). there will of course be the normal analog circuit start-up and settling time.

Wake-up from standby.
To re-activate the chipset from its "standby" state one simply sends a "null" control word (Two bytes of any data). The data contained in the first word will be ignored.
The first byte (8bits) are used as an interrupt - to wake the State Machine an 8bit byte ensures there is sufficient time for the internal oscillator to start and stabilize.
The second byte is used to clear the control word buffer.
The State Machine will then enable the external osc
The external oscillator\or output to the dpASP ACLK pin wakes up the dpASP
The RFID State Machine OSCen will become active 1milli-second after the last bit of the Control word arrives at the State Machine.

External Oscillator start-up (will depend on the Oscillator used), Anadigm AN238K04 Evaluation board the Oscillator module starts in less than 50usec.

RFID State Machine BUSY pin.
This pin indicates when the state machine is busy configuring the AN238E04 device
At start-up (power up) BUSY pin will drive high whilst the chipset is configuring, start-up configuration time is approx 36msec. When configuration has completed this pin pulls low.
When a re-configuration word is received this pin will drive high until board configuration is complete, the time taken for the board to reconfigure itself after a new control word can be anything from 1 to 50msec.
1msec for a small parameter change (e.g. changing the first stage gain),
Up to 50msec, for changing from circuit to circuit, (e.g. RFID_wide to RFID_twin).
For simplicity between control words should be at least 50msec,
Except when the first control word is a “wake-up” in which case there should be a delay of just 30us before the next control word is entered.
Note that the BUSY signal will drive high after each control word is entered to indicate that the system is busy. When BUSY goes low, it is safe to enter another control word.

Analog signal path in the AN238E04has an additional start-up delay
When changing circuit parameters the Analog signal path will be reconfigured immediately after the busy line drives low.
At start-up, following Reset and when changing circuits (e.g. from “wide” to “twin”, the Analog signal path within the AN238E04 device will be active 55msec after the State Machine (AN238C04) busy line drives low.

1.8 RFID STATE MACHINE ELECTRICAL CHARACTERISTICS

Parameter	Absolute Maximum Ratings	Unit
Ambient temperature under bias	-40 to +125	°C
Storage temperature	-65 to +150	°C
Voltage on VDD with respect to VSS	-0.3 to +4.5 (nominal 3.3volts)	V
Voltage on any pin with respect to VSS	-0.3 to (VDD + 0.3)	V
Total power dissipation (Note 1)	0.5	W
Maximum current out of VSS pin	300	mA
Maximum current into VDD pin	250	mA
Input clamp current, (Vin < 0 or Vin > VDD)	±20	mA
Output clamp current, (Vout < 0 or Vout > VDD)	±20	mA
Maximum output current sunk by any I/O pin	25	mA
Maximum output current sourced by any I/O pin	25	mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD – ∑ IOH} + ∑ {(VDD – VOH) x IOH} + ∑(VOL x IOL)

Parameter	Typical	Unit
Typical Supply current	0.35	mA
The RFID State Machine has an internal 8MHz clock.	Fosc = 8.0 +/- 1%	MHz
CLRb Minimum pulse width	2	usec
Internal Osc startup time	128	usec

1.9 RFID dpASP

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	VDD	-0.5	-	3.6	V	AVSS, BVSS, DVSS and SVSS all held to 0.0 V [a]
xVDD to xVDD Offset		-0.5		0.5	V	Ideally all supplies have the same voltage
Package Power Dissipation	Pmax 25°C 85°C	-	-	 4.5 1.8	W	Still air, No heatsink, 4 layer board, 44 pins. θja = 55°C/W
AN238E04 max power dissipation	FPAAmax	-	-	0.25	W	Maximim power dissipation all resources used,
Any Pin Input Voltage	Vinmax	Vss-0.5	-	Vdd+0.5	V	
Ambient Operating Temperature	Top	-40	-	85	°C	
Storage Temperature	Tstg	-65		125	°C	

[a] Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for Vdd of up to 4.0 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	3.0	3.3	3.6	V	V	AVSS, BVSS, DVSS and SVSS all held to 0 V
Analog Input Voltage.	VMR -1.375	-	VMR +1.375	V	V	VMR is 1.5 volts above AVSS
Digital Input Voltage	0	-	DVDD	V	V	
Junction Temp	-40	-	125	°C	°C	Assume a package θja = 55°C/W [b]

[b] To calculate the junction temperature (Tj) you must first empirically determine the current draw (total Idd) for the design. The programmable nature of this device means this can vary by orders of magnitude between different circuit designs. Once the current consumption is established then the following formula can be used; Tj = Ta + Idd x VDD x 22.5 °C/W, where Ta is the ambient temperature. Worst case θja = 22.5 °C/W assumes no air flow and no additional heatsink, 44 pads and the exposed die pad soldered to PCB.

Typical Operating

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	VDD	-	3.3	-	V	AVSS, BVSS, DVSS and SVSS all held to 0.0 V
Power consumption	P1	-	160 (135)	-	mW	RFID_wide (without Notch filter)
Power consumption	P2	-	160	-	mW	RFID_twin
Power consumption	P3	-	190	-	mW	RFID_triple
Power consumption	P4	-	155	-	mW	RFID_fast
Power consumption	P5	-	1.0	-	mW	Standby mode

Analog Inputs General

All analog signal processing within the device is done with respect to Voltage Main Reference (VMR) which is nominally 1.5 V. The VMR signal is derived from a high precision, temperature compensated bandgap reference source.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High Precision Input Range [c]	Vina	0.125	-	2.845	V	VMR +/- 1.375v
Standard Input Range [d]	Vina	0.05	-	2.95	V	VMR +/- 1.45v
Common Mode Input Range	Vcm	1.4	1.5	1.6	V	
Input Offset	Vos	-	300	500	uV	This is auto nulled
Input Frequency	Fain	0	1	4	MHz	
Input impedance	Rin	1	-	-	Mohms	RangeMaster is designed to have an a.c. coupled input.

[c.] High precision operating range provides optimal linearity and dynamic range.

[d.] Standard precision operating range provides maximum dynamic range and reduced linearity.

Analog Outputs

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High Precision Output Range [c]	Vouta	0.125	-	2.875	V	VMR +/- 1.375v
Standard Output Range [d]	Vouta	0.05	-	2.95	V	VMR +/- 1.45v
Differential Output [c]	Vdiffouta	-	-	+/-2.75	V	Common mode voltage = 1.5 V
Common Mode Voltage	Vcm	1.4	1.5	1.6	V	
Output Impedance	Rout	-	33	-	Ohms	Measured at package pins. Track impedance increases the effective output impedance. The OpAmp is designed to drive all internal nodes,
Output Load, External	Rload	1	10	-	Kohm	This device is not intended to drive loads, connect to a buffer Amp or ADC input
Output Load, External	Cload	-	-	100	pF	

[c]. High precision operating range provides optimal linearity and dynamic range.

[d]. Standard precision operating range provides maximum dynamic range and reduced linearity.

General Digital Output Characteristics (Vdd = 3.3v +/- 10%, -40 to 85 deg.C)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Voltage Low	Vol	0	-	20	-	% of DVDD
Output Voltage High	Voh	80	-	100	-	% of DVDD
Max. Capacitive Load	Cmax	-	-	10	pF	The maximum load for a digital output is 10 pF // 10 Kohm
Min. Resistive Load	Rmin	10	-	-	Kohm	The maximum load for a digital output is 10 pF // 10 Kohm
DCLK Frequency	Fmax	0	-	8	MHz	DCLK is fixed for the RFID chipset
ACLK Frequency	Fmax	24	-	24	MHz	The ACLK frequency is fixed for the RFID dpASP
Clock Duty Cycle	-	45	-	55	%	All clocks

RFID ACLK

The RFID dpASP device's requires an external clock that must be 24 MHz.

1.10 MECHANICAL AND HANDLING

The RangeMaster2 is a two-chip solution. The RFID dpASP is packaged in industry standard 44 lead QFN package and the RFID state machine is packaged in an industry standard 20-pin SSOP. The following pages detail the Pin configuration and the mechanical package details.

Dry pack handling is recommended. The packages are qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.

ESD Characteristics RFID dpASP, AN238E04

Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital Inputs	4000V	250V	4kV
Digital Outputs	4000V	250V	4kV
Digital Bidirectional	4000V	250V	4kV
Digital Open Drain	4000V	250V	4kV
Analog Inputs	2000V	200V	4kV
Analog Outputs	1500V	100V	4kV
Reference Voltages	1500V	100V	4kV

The AN238E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN238E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ESD Characteristics RFID State Machine AN238C04

Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital Inputs	4000V	250V	4kV
Digital Outputs	4000V	250V	4kV
Digital Bidirectional	4000V	250V	4kV
Digital Open Drain	4000V	250V	4kV

The AN238C04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN238C04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

RFID dpASP PINOUT, 44pin QFN.

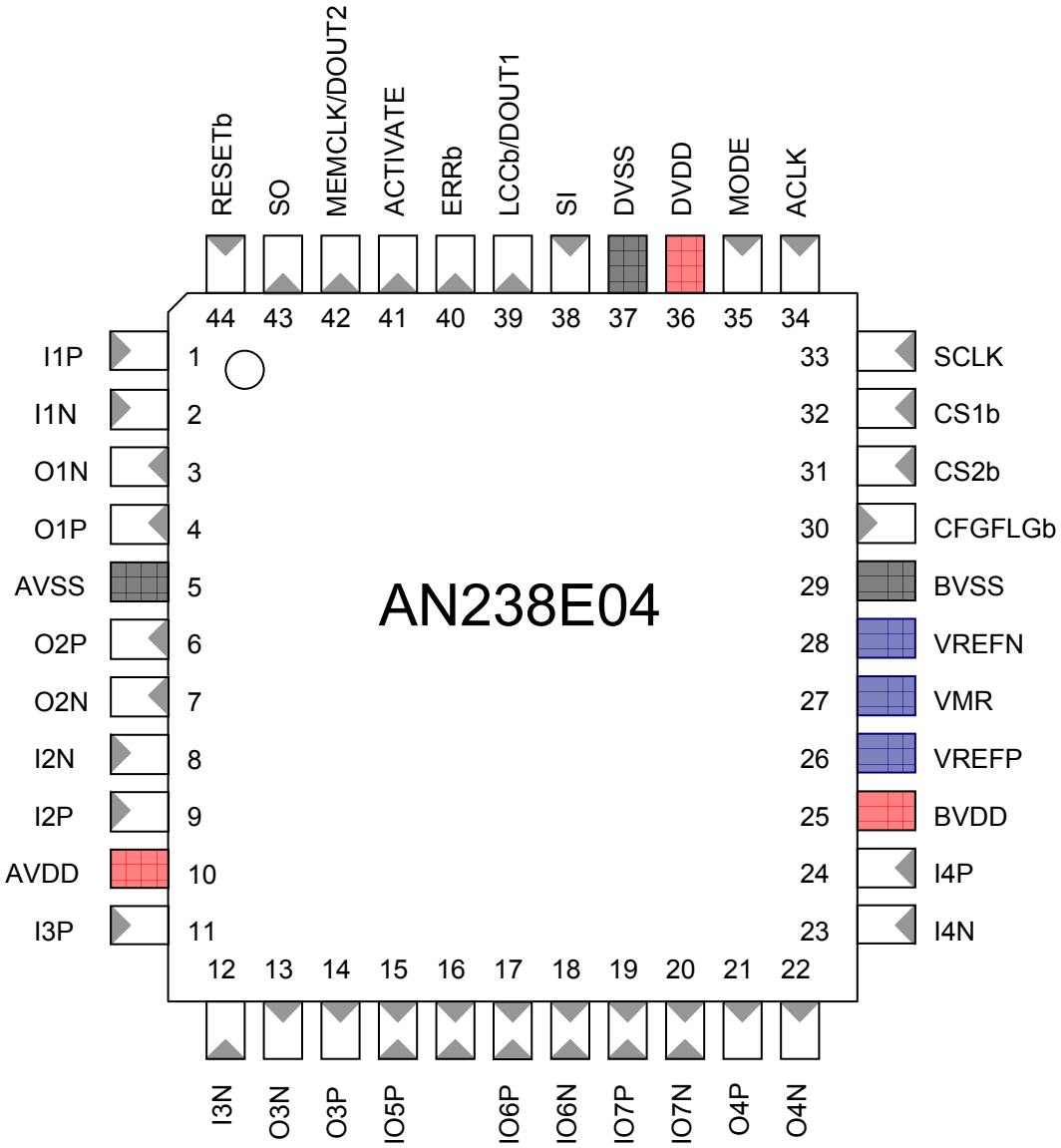


Fig 7, RFID dpASP Pin drawing

Pin No.	RFID dpASP Pin name	Generic Pin Name	Pin Type	Comments
1	*Not used*	I1P	+ve Input	Do not make an electrical connection, leave Not Connected
2	*Not used*	I1N	-ve Input	
3	O1N	O1N	-ve Output	Inverted Digital output from comparator
4	O1P	O1P	+ve Output	Digital output from comparator
5	AVSS	AVSS	Ground Supply	Analog ground, 0 Volts
6	O2P	O2P	+ve Input	Differential Analog output from RangeMaster2 signal path, For single-ended use O2P and leave O2N not connected.
7	O2N	O2N	-ve Input	
8	*Not used*	I2N	-ve Output	Do not make an electrical connection, leave Not Connected
9	*Not used*	I2P	+ve Output	
10	AVDD	AVDD	Positive Supply	Analog power 3.3 Volts
11	I3P	I3P	+ve Input	Differential Analog input to RangeMaster2 signal path, For single-ended use I3P and connect I3N to VMR
12	I3N	I3N	-ve Input	
13	*Not used*	O3N	-ve Output	Do not make an electrical connection, leave Not Connected
14	*Not used*	O3P	+ve Output	
15	*Not used*	IO5P	+ve Input/Output	Do not make an electrical connection, leave Not Connected
16	*Not used*	IO5N	-ve Input/Output	
17	*Not used*	IO6P	+ve Input/Output	Do not make an electrical connection, leave Not Connected
18	*Not used*	IO6N	-ve Input/Output	
19	ON/OFFb	IO7P	+ve Input/Output	Input to control Anti-saturation switches
20	IO7N	IO7N	-ve Input/Output	Connect to VMR
21	*Not used*	O4P	+ve Input	Do not make an electrical connection, leave Not Connected
22	*Not used*	O4N	-ve Input	
23	*Not used*	I4N	-ve Output	
24	*Not used*	I4P	+ve Output	
25	BVDD	BVDD	Positive Supply	Voltage reference power 3.3 Volts
26	VREFP	VREFP	Reference load	Reference Voltage Noise suppression. Connected a 100nF capacitor from each pin to BVSS. The capacitive reservoir is used to sink and source peak current, thus reducing noise and maintaining stable reference voltages.
27	VMR	VMR	Reference load	
28	VREFN	VREFN	Reference load	
29	BVSS	BVSS	Ground Supply	Voltage reference ground 0 Volts
30	*Not used*	CFGFLGb	Digital Output	Config status pin. Open Drain Output with internal Pull-up resistor Do not make an electrical connection, leave Not Connected
31	CS2b	CS2b	Digital input	Chip select pin,
32	CS1b	CS1b	Digital input	Device select
33	SCLK	SCLK	Digital input	CMOS, configuration logic strobe clock.
34	ACLK	ACLK	Digital input	CMOS, Analog clock input, for RangeMaster2 must be 24MHz
35	MODE	MODE	Digital input	Connect to VSS (ACLK and SCLK sourced externally).
36	DVDD	DVDD	Positive Supply	Digital power 3.3 Volts
37	DVSS	DVSS	Ground Supply	Digital ground 0.0 Volts
38	SI	SI	Digital input	CMOS Serial data input.
39	*Not used*	LCCb/ DOUT1	Digital output	CMOS. Default function, Indicates Local Configuration Complete. Do not make an electrical connection, leave Not Connected
40	ERRb	ERRb	Digital output	Error indication. Open Drain, External Pull-up resistor must be used (10KOhms)
41	ACTIVATE	ACTIVATE	Digital Output	Indicates Device activation. Open Drain Output with an internal Pull-up resistor. The output voltage is also sensed by internal circuitry,
42	*Not used*	MEMCLK/ DOUT2	Digital Output	Do not make an electrical connection, leave Not Connected Used by Anadigm on Evaluation boards for board test.
43	*Not used*	SO	Digital Output	Do not make an electrical connection, leave Not Connected.
44	RESETb	RESETb	Digital Input	Connected to VSS to reset the FPAA. If held low the FPAA will remain in reset (30msec delay internal set-up time follows release of RESETb (when this pin is pulled high))

Table 1, RFID dpASP Pin list

Package Outline Drawing, 44L QFN, (7.0 x 7.0 x0.9 mm)

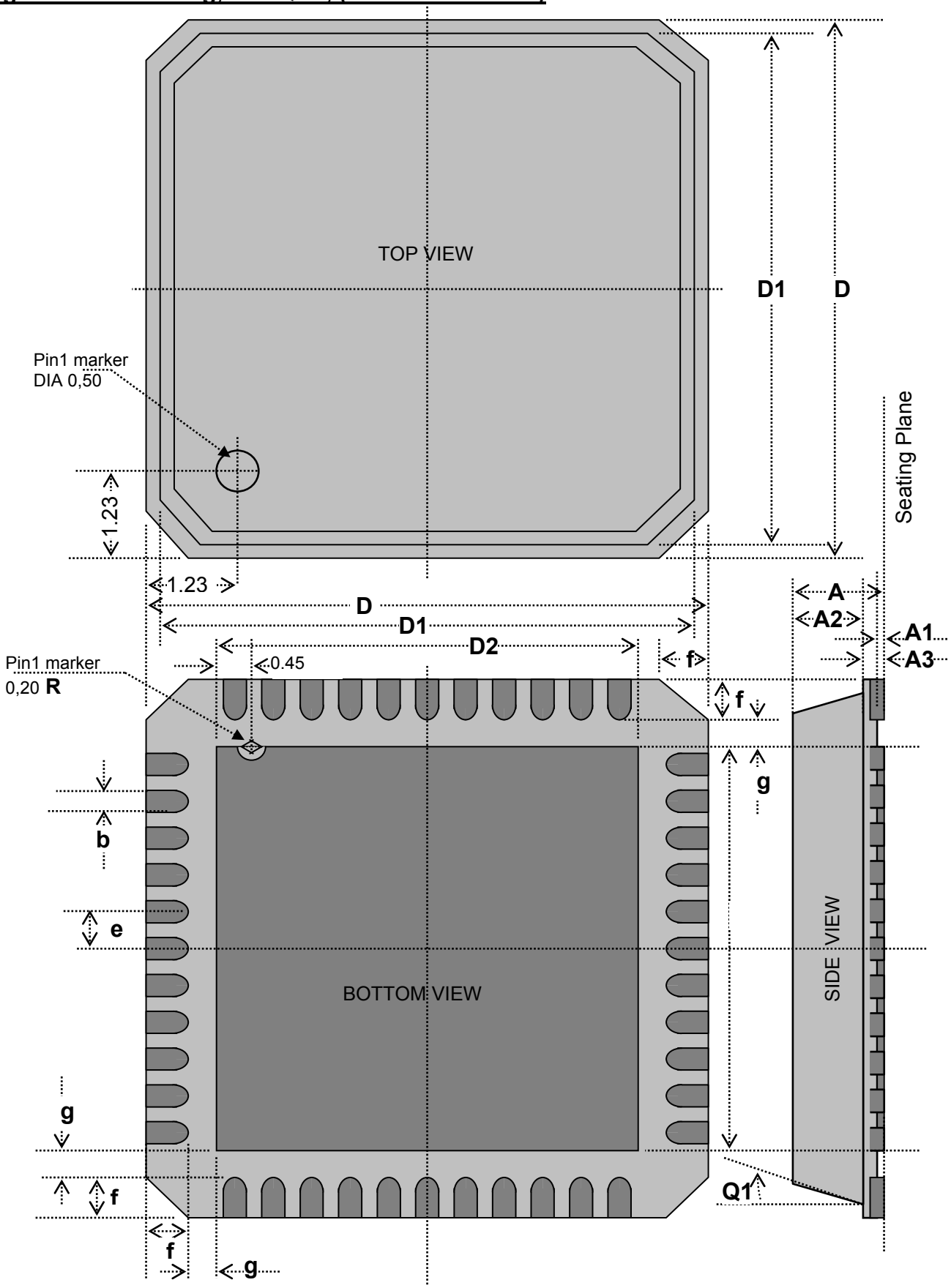
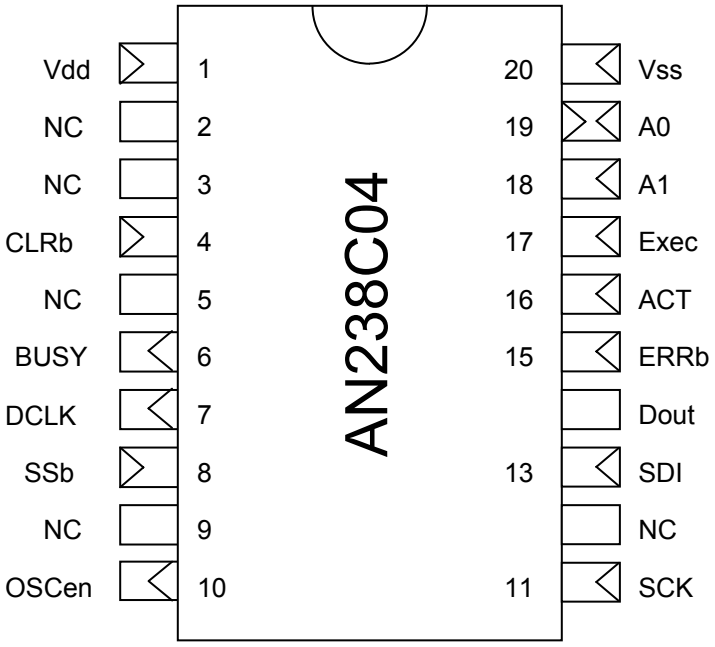


Figure 8: Package drawing for the RangeMaster2 RFID State Machine (AN238C04)

All dimension are in mm.

Symbol	Min	Nom	Max
A	-	-	0.90
A1	0.00	0.01	0.05
A2	-	0.65	0.70
A3	-	0.20	-
D	-	7.00	-
D1	-	6.75	-
D2	5.30	5.50	5.70
b	0.20	0.25	0.32
e	-	0.50	-
f	0.26	0.42	0.60
g	0.2	-	-
Q1	0.0’	(Ang.deg.)	12’
R	0.09	-	-

1.11 RFID STATE MACHINE PINOUT, 20 Pin SSOP,



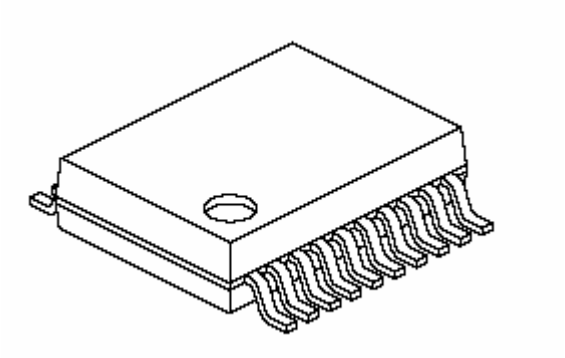
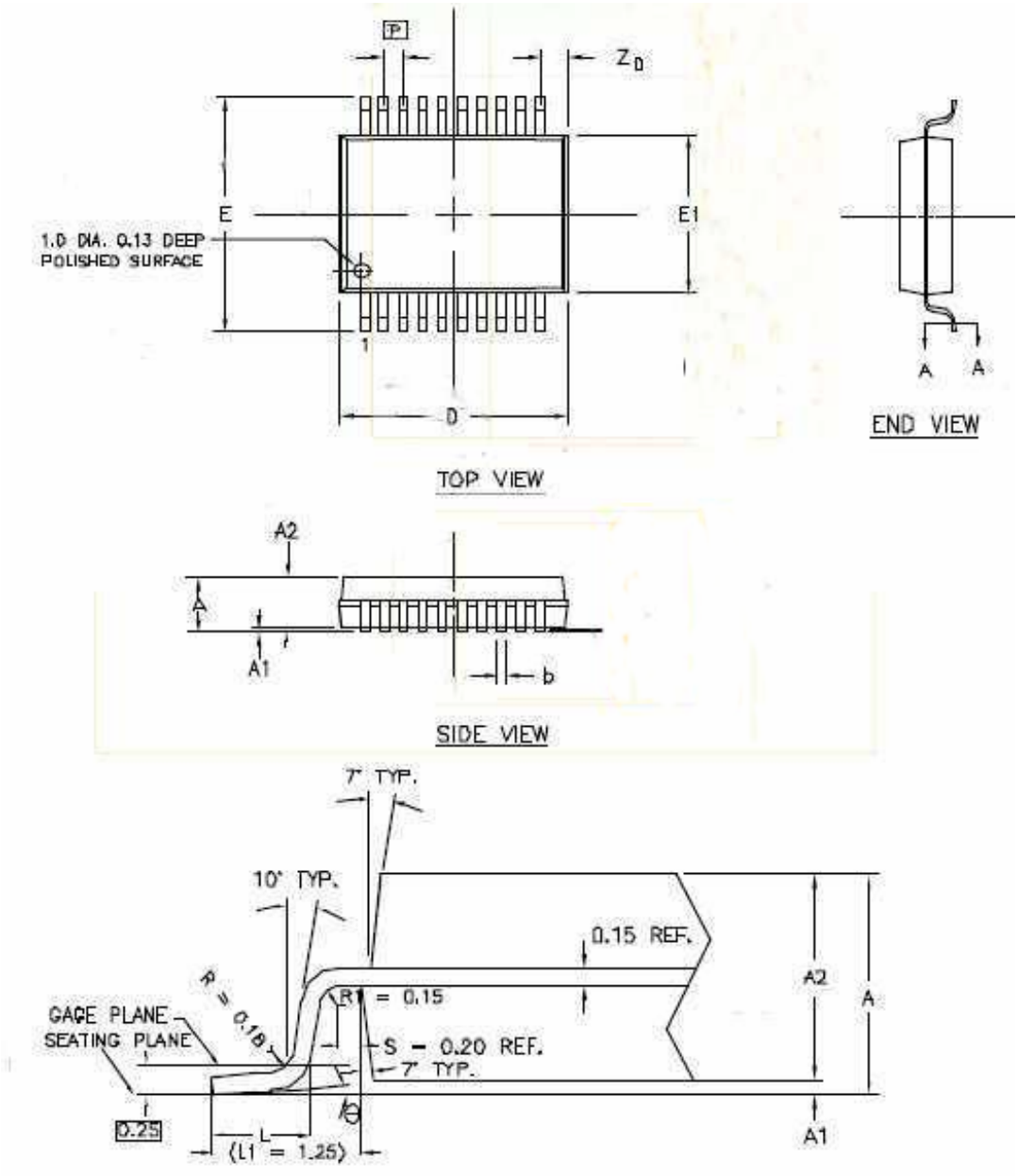


Fig 9, RFID State Machine Pin drawing

Pin Number	Pin Name	Pin Type	Description
1	Vdd	Supply	Positive 5v supply
2	NC	n/a	Do not make an electrical connection, leave Not Connected
3	NC	n/a	Do not make an electrical connection, leave Not Connected
4	CLRb	Input	CMOS level Schmitt trigger with internal Pull-up, State Machine Clear,
5	NC	n/a	Do not make an electrical connection, leave Not Connected
6	Busy	Output	Busy output indication, the state machine is unable to accept serial data when this pin is high. At start-up will drive high whilst the chipset is configuring, start-up configuration time is approx 36msec. When configuration has completed this pin pulls low. When a re-configuration word is received this pin will drive high until chipset configuration is complete. Maximum busy time = 50msec.
7	DCLK	Output	CMOS output, Data strobe Clock to RFID dpASP
8	SSb	Input	Slave Select Input
9	NC	n/a	Do not make an electrical connection, leave Not Connected
10	OSCen	Output	Logic high level used to enable external; oscillator module, logic low used to disable same oscillator module during “standby” to minimize current.
11	SCK	Input	SPI compatible Clock input, CMOS level.
12	NC	n/a	Do not make an electrical connection, leave Not Connected
13	SDI	Input	SPI compatible Serial Data In, CMOS level Schmitt trigger
14	Dout	Output	CMOS output, Data out to RFID dpASP
15	ERRb	Input	CMOS level Schmitt trigger,
16	ACT	Input	CMOS level
17	Exec	I/O	CMOS level, this pin is functionally disabled in this Device.
18	A1	n/a	Factory reserved, test pin, leave Not Connected
19	A0	n/a	Factory reserved, test pin, leave Not Connected
20	Vss	Supply	Power supply Ground (Zero Volts)

Table2, RFID State Machine Pin drawing

20-Lead Plastic Shrink Small Outline (SSOP) – 209 mil Body, 5.30 mm. Lead finish Matt tin (Sn).



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95

Figure 10: Package drawing for the RangeMaster2 RFID State Machine (AN238C04)

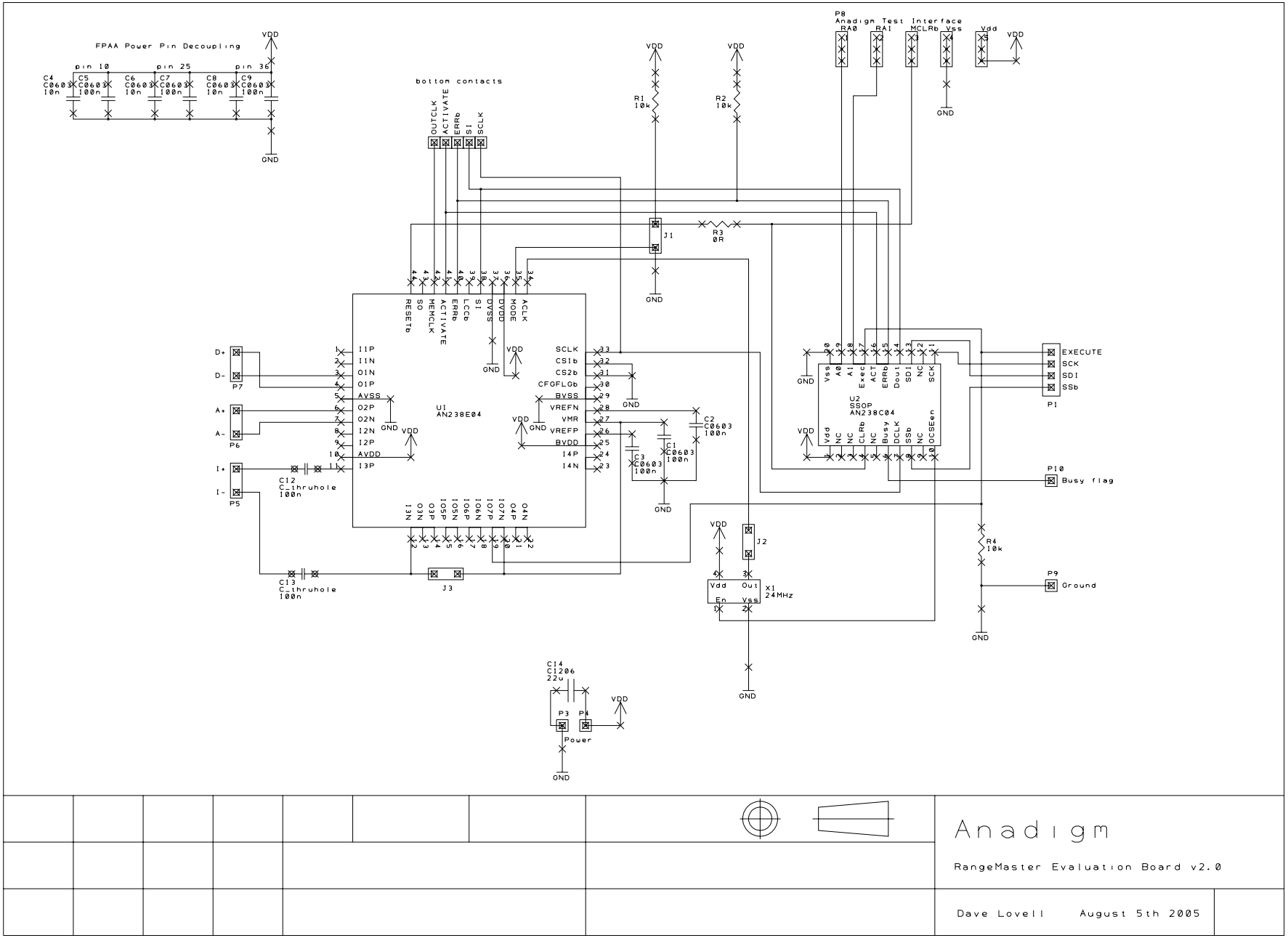


Figure 11, RangeMaster2 Evaluation Board Schematic diagram.